Design Example Report

Title	***10 W Dual Output Power Supply Using InnoSwitch™3-EP 900 V INN3692C-H606***
Specification	90 VAC – 420 VAC Input; 5 V, 0.3 A and 12 V, 0.7 A Outputs
Application	Dual Output Open Frame Industrial Power Supply
Author	Application Engineering Department
Document Number	DER-745
Date	July 21, 2022
Revision	1.1

Summary and Features

- InnoSwitch3-EP 900 V - industry first AC/DC ICs with isolated, safety rated integrated feedback, 900 V MOSFET
- Built in synchronous rectification for >85% efficiency at nominal AC input
- All the benefits of secondary side control with the simplicity of primary side regulation
  - Insensitive to transformer variation
  - Extremely fast transient response independent of load timing
- Meets output cross regulation requirements without linear regulators
- Primary sensed output overvoltage protection (OVP) eliminates optocoupler for fault protection
- Accurate thermal protection with hysteretic shutdown
- Input voltage monitor with accurate brown-in / brown-out and overvoltage protection

Power Integrations

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Table of Contents

Important Note:
Although this board is design to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should perform using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This document is an engineering report describing a 0.3 A, 5 V and 0.7 A, 12 V dual output embedded power supply utilizing INN3692C-H606 from the InnoSwitch3-EP family of ICs.

This design shows the high power density and efficiency that is possible due to the high level of integration while still providing exceptional performance.

The document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

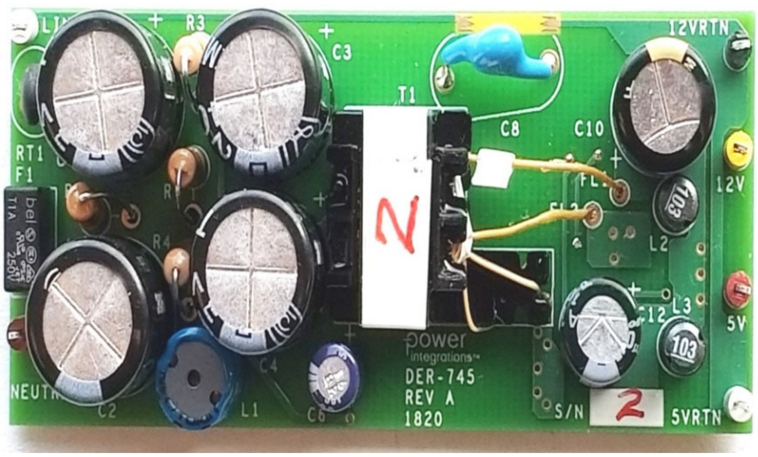


Figure 1 – Populated Circuit Board Photograph, Top.

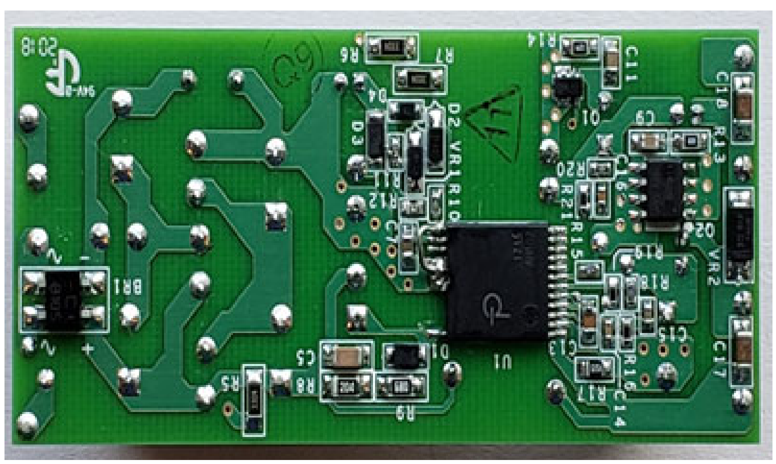


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		420	VAC	2 Wire Input.
Frequency	f_{LINE}	47	50/60	63	Hz	
Output						
Output Voltage 1	V_{OUT1}	4.75	5	5.25	V	±5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			50	mV	20 MHz Bandwidth.
Output Current 1	I_{OUT1}	0		0.3	A	
Output Voltage 2	V_{OUT2}	10.2	12	13.8	V	±15 %, (±10% with 10% Min Load on 12 V.)
Output Ripple Voltage 2	$V_{RIPPLE2}$			120	mV	20 MHz Bandwidth.
Output Current 2	I_{OUT2}	0		0.7	A	
Total Output Power						
Continuous Output Power	P_{OUT}			10	W	
Efficiency						
Full Load	η	85			%	Measured at 110 / 230 VAC, P_{OUT} 25 ºC.
No Load Input Power				30	mW	V_{IN} at 230 VAC. (Without Voltage Balancing Resistors for Input Capacitors)
Environmental						
		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC950, UL1950 Class II				
Surge Differential		1			kV	1.2/50 µs Surge, IEC 1000-4-5, Series Impedance: Differential Mode: 2 Ω.
Surge Common mode Ring Wave		2			kV	100 kHz Ring Wave, 12 Ω Common Mode.
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level.

3 Schematic

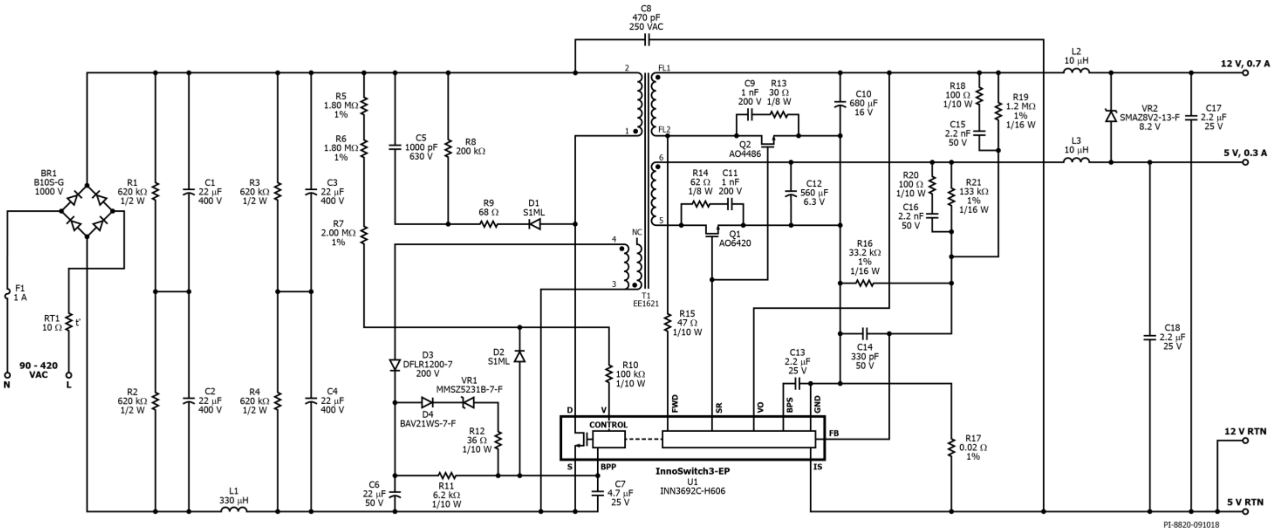


Figure 3 – Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

Fuse F1 isolates the circuit and provides protection from component failure and thermistor RT1 limits inrush current and for surge protection. Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the filter consisting of C1, C2, C3 and C4. The differential inductance of L1 with capacitors C1, C2, C3, and C4 provide differential noise filtering. Resistors R1, R2, R3 and R4 function to balance the voltage between the bulk capacitors in series.

4.2 *InnoSwitch3-EP Primary*

One side of the transformer primary is connected to the rectified DC bus, the other is connected to the integrated 900 V power MOSFET inside the InnoSwitch3-EP 900 V IC (U1).

A low cost RCD clamp formed by D1, R8, R9, and C5 limits the peak drain voltage due to the effects of transformer leakage inductance.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor, C7, when AC is first applied. During normal operation, the primary side block is powered from an auxiliary winding on the transformer, which is configured as a flyback winding. The output is rectified and filtered using diode D3 and capacitor C6, and it fed in the BPP pin via a current limiting resistor R11. The primary side overvoltage protection is obtained using Zener diode VR1. In the event of overvoltage at output, the increased voltage at the output of the bias winding cause the Zener diode VR1 to conduct and triggers the OVP latch in the primary side controller of the InnoSwitch3-EP 900 V IC.

Resistor R5, R6, and R7 provide line voltage sensing and provide a current to U1, which is proportional to the DC voltage across capacitors, C3 and C4. At approximately 650 VDC the current through these resistors exceeds the line over-voltage threshold, which results in disabling of U1. The current limiting resistor R10 disables UV function by providing a fixed current into Vpin from BPP voltage through D2.

4.3 *InnoSwitch3-EP IC Secondary*

The secondary side of the InnoSwitch3-EP 900 V provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification.

Total output current is sensed by R17 between the IS and GND pins with a threshold of approximately 35 mV to reduce losses. Once the current sense threshold is exceeded for longer than fixed time (t_{AR}), the device enters auto-restart (AR) in the event of output short-circuit. Output rectification for the 5 V output is provided by SR FET Q1. Very low ESR capacitor C12 provides filtering, and inductor L3 and capacitor C18 form a second stage filter that significantly attenuates the high frequency ripple and noise at the 5 V output. Output rectification for the 12 V output is provided by SR FET Q2. Very low ESR capacitors C10 provides filtering, and Inductor L2 and capacitor C17 form a second stage filter that significantly attenuates the high frequency ripple and noise at the 12 V output.

RC snubber networks comprising R14 and C11 for Q1, R13 and C9 for Q2 damp high frequency ringing across SR FETs, which results from leakage inductance of the transformer windings and the secondary trace inductances.

The gates of Q1 and Q2 are turned on based on the winding voltage sensed via R15 and the FWD pin of the IC. In continuous conduction mode operation, the power MOSFET is turned off just prior to the secondary side controller commanding a new switching cycle from the primary. In discontinuous mode the MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold ($V_{SR(TH)}$). Secondary side control of the primary side MOSFET ensure that it is never on simultaneously with the synchronous rectification MOSFET. The MOSFET drive signal is output on the SR pin.

The secondary side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. The output voltage powers the device, and it fed into the VO pin and charges the decoupling capacitor C13 and an internal regulator. The unit enters auto-restart when the sensed output voltage is lower than 3 V.

Resistor R19, R21 and R16 form a voltage divider network that senses the output voltage from both outputs for better cross-regulation. Zener diode VR2 improves the cross regulation when only the 5 V output is loaded, which results in the 12 V output operating at the higher end of the specification. The InnoSwitch3-EP IC has an internal reference of 1.265 V. Feedback compensation networks comprising capacitors C15, C16 and resistors R18, R20 reduce the output ripple voltage. Capacitor C14 provides decoupling from high frequency noise affecting power supply operation.

5 PCB Layout

PCB copper thickness is 2 oz (2.8 mils / 71 μm) unless otherwise stated.

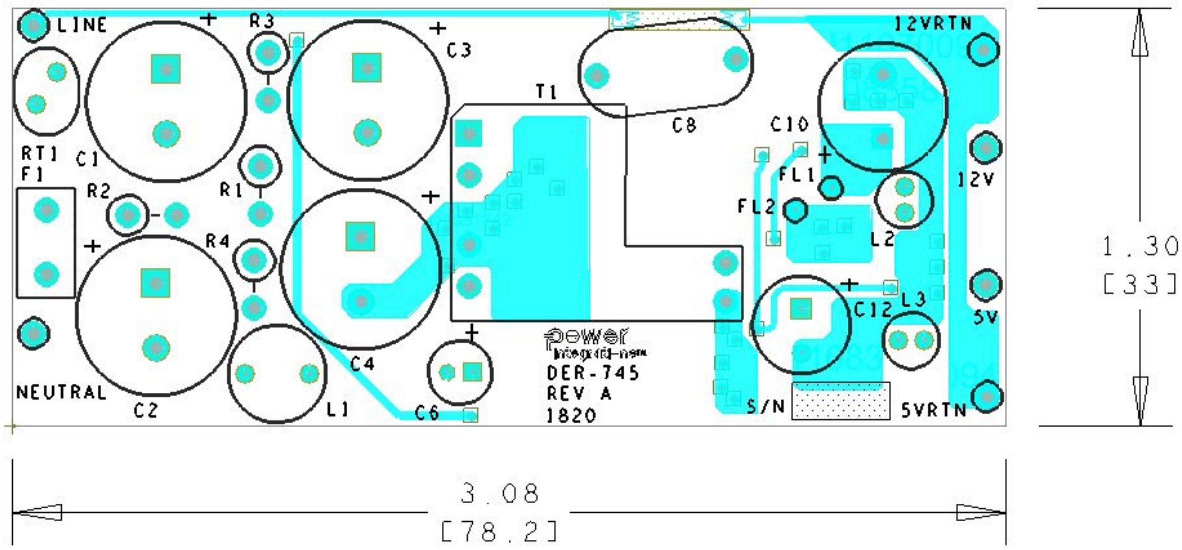


Figure 4 – Top.

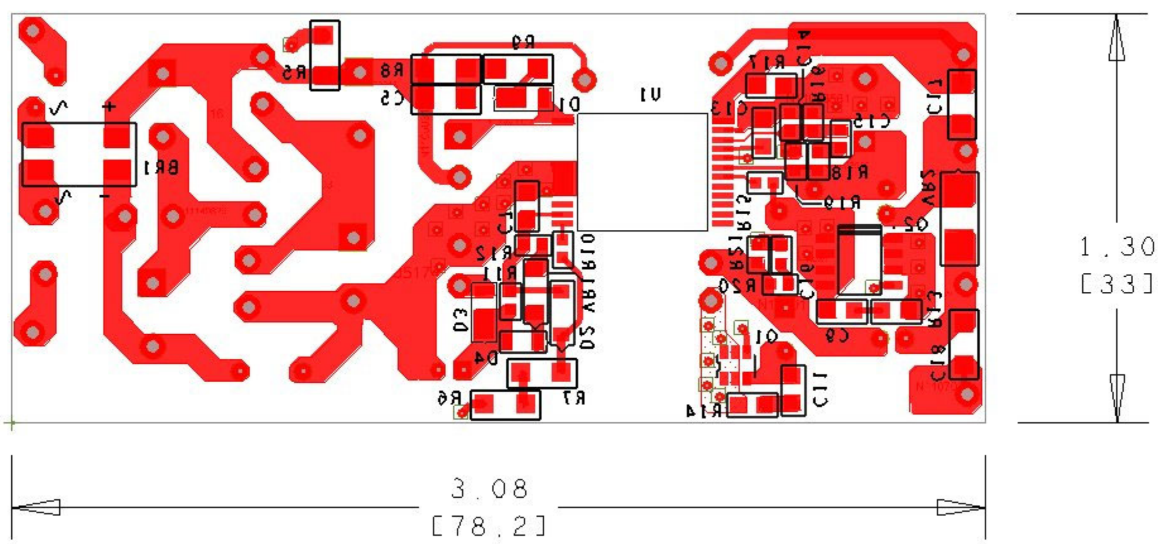


Figure 5 – Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rect, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	4	C1 C2 C3 C4	22 μF, 400 V, Electrolytic, (12.5 x 16)	TYB2GM220J160	Ltec
3	1	C5	1000 pF, 630 V, Ceramic, X7R, 1206	C1206C102KBRACTU	Kemet
4	1	C6	22 μF, 50 V, Electrolytic, (5 x 11)	UPW1H220MDD	Nichicon
5	1	C7	4.7 μF, ±10%, 25 V, Ceramic, X7R, -55°C ~ 125°C, 0805	TMK212AB7475KG-T	Taiyo Yuden
6	1	C8	470 pF, 500 VAC, Film, X1Y1	WKP471MCPEF0KR	Vishay
7	2	C9 C11	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
8	1	C10	680 μF, 16 V, Electrolytic, Radial, Low ESR, 26 mΩ, (10 x 16)	EEU-FM1C681	Panasonic
9	1	C12	ALUM ULTRA LOW IMPEDANCE, 560 uF, 20%, 6.3 V, 3000 Hrs @ 105°C (8x11)	6.3ZLG560MEFC8X11.5	Rubycon
10	1	C13	2.2 μF, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M	TDK
11	1	C14	330 pF 50 V, Ceramic, X7R, 0603	CC0603KRX7R9BB331	Yageo
12	2	C15 C16	2.2 nF 50 V, Ceramic, X7R, 0603	C0603C222K5RACTU	Yageo
13	2	C17 C18	2.2 μF, 25 V, Ceramic, X7R, 1206	TMK316B7225KL-T	Taiyo Yuden
14	2	D1, D2	1 kV, 1 A, Standard Recovery, SMA	S1ML	TAIWAN SEMI
15	1	D3	200 V, 1 A, Rect, Glass Passivated, POWERDI123	DFLR1200-7	Diodes, Inc.
16	1	D4	250 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV21WS-7-F	Diodes, Inc.
17	1	F1	1 A, 250 V, Slow, Long Time Lag, RST 1	RST 1	Belfuse
18	2	FL1 FL2	Flying Lead, Hole size 30 mils	N/A	N/A
19	1	L1	330 μH, 0.55 A, 9 x 11.5 mm	SBC3-331-551	Tokin
20	2	L2 L3	Inductor, 10 μH, Unshielded, Wirewound, 950 mA, 140 mΩ Max, Radial	11R103C	Murata
21	1	Q1	MOSFET, N-CH, 60V, 4.2 A, 6TSOP	AO6420	Alpha & Omega Semi
22	1	Q2	MOSFET, N-CH, 100 V, 4.2 A (Ta), 3.1W (Ta), 79 mΩ @ 3 A, 10 V,8SOIC	AO4486	Alpha & Omega Semi
23	4	R1 R2 R3 R4	RES, 620 kΩ, 5%, 1/2 W, Carbon Film	CFR-50JB-620K	Yageo
24	2	R5 R6	RES, 1.80 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1804V	Panasonic
25	1	R7	RES, 2.00 MΩ, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
26	1	R8	RES, 200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
27	1	R9	RES, 68 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ680V	Panasonic
28	1	R10	RES, 100 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ104V	Panasonic
29	1	R11	RES, 6.2 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ622V	Panasonic
30	1	R12	RES, 36 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ360V	Panasonic
31	1	R13	RES, 30 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ300V	Panasonic
32	1	R14	RES, 62 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ620V	Panasonic
33	1	R15	RES, 47 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
34	1	R16	RES, 33.2 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF3322V	Panasonic
35	1	R17	RES, 0.02 Ω, 1%, 1/4 W, Thick Film, 0805	RL0805FR-7W0R02L	Yageo
36	2	R18 R20	RES, 100 Ω, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ101V	Panasonic
37	1	R19	RES, 1.20 MΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1204V	Panasonic
38	1	R21	RES, 133 kΩ, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1333V	Panasonic
39	1	RT1	NTC Thermistor, 10 Ω, 0.7 A	MF72-010D5	Cantherm
40	1	T1	Bobbin, EE1621, Vertical, 8 pins, 4pri, 4sec Transformer	EE-1621 POL-INN055	Shen Zhen Xin Yu Jia Premier Magnetics
41	1	U1	InnoSwitch3-EP Integrated Circuit, InSOP24D	INN3692C-H606	Power Integrations
42	1	VR1	Diode, Zener 5.1 V 500 mW SOD123	MMSZ5231B-7-F	Diodes, Inc.
43	1	VR2	Diode, Zener, 8.2 V, ±5%, 1W, DO-214AC, SMA	SMAZ8V2-13-F	Diodes, Inc.
44	1	12V	Test Point, PC MINI, .040"(1.02 mm)D, YEL, TH	5004	Keystone
45	1	12VRTN	Test Point, BLK, Miniature TH MOUNT	5001	Keystone
46	2	5V NEUTRAL	Test Point, RED, Miniature TH MOUNT	5000	Keystone
47	2	5VRTN LINE	Test Point, WHT, Miniature TH MOUNT	5002	Keystone

7 Transformer Specification

7.1 *Electrical Diagram*

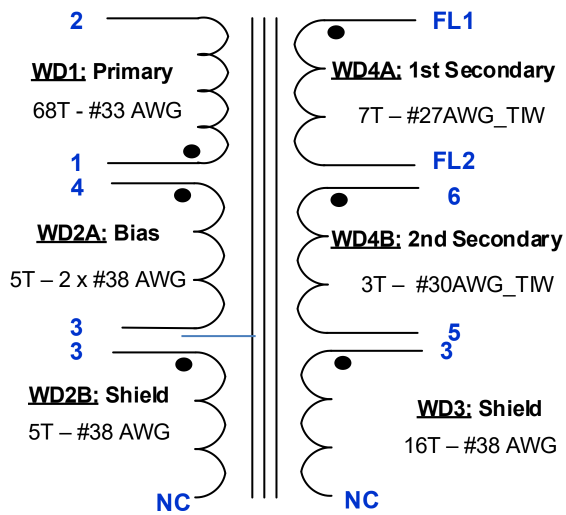


Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specifications*

Parameter	Condition	Spec.
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 1 and 2, with all other windings open.	1180 µH ±7%
Primary Leakage Inductance	Between pin 1 and 2, with FL1, FL2, 5, 6 shorted.	40 µH (Max).

7.3 *Material List*

Item	Description
[1]	Core: EE1621; Hong Kong Magnetics, ME 95 or Equivalent; Gapped for ALG of 218nH/T².
[2]	Bobbin: EE1621-Vertical – 8pins (4/4), SHEN ZEN XIN YU JIA Technology LTD.
[3]	Magnet Wire: #33 AWG, Double Coated.
[4]	Magnet Wire: #38 AWG, Double Coated.
[5]	Magnet Wire: #27 AWG, Triple Insulated Wire.
[6]	Magnet Wire: #30 AWG, Triple Insulated Wire.
[7]	Barrier Tape: 3M 1298 Polyester Film, 1 mil Thickness, 5.5 mm Wide.
[8]	Copper Foil: 2 mil Thick, 4.0 mm x 20.0 mm.
[9]	Tape: 3M Polyester Film, 1 mil Thick, 7 mm Wide.
[10]	Varnish: Dolph BC-359.

7.4 *Transformer Build Diagram*

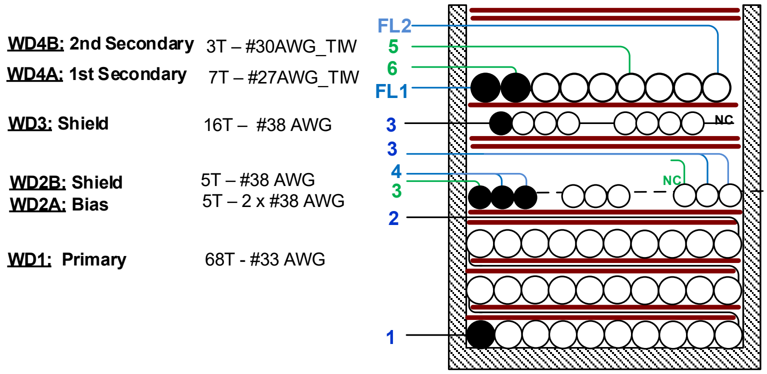
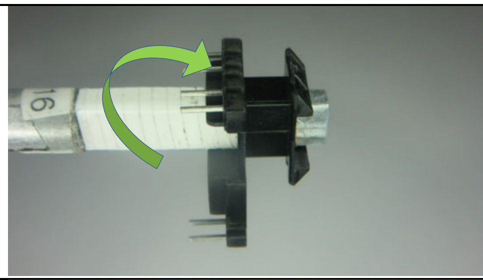
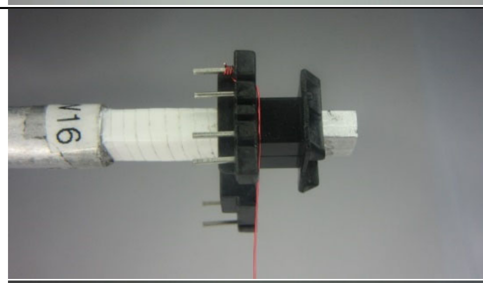
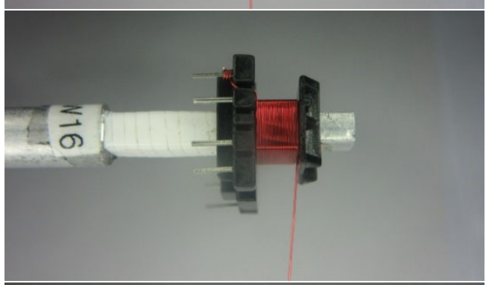
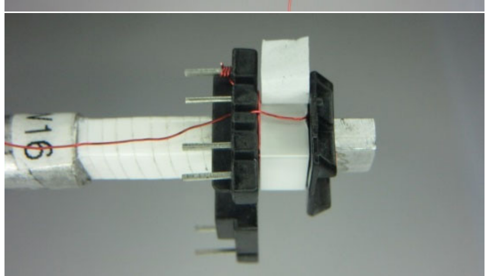
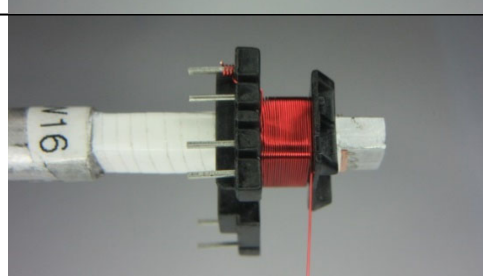
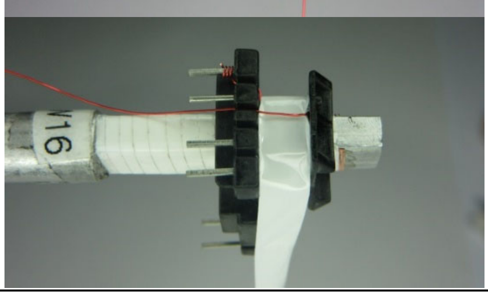


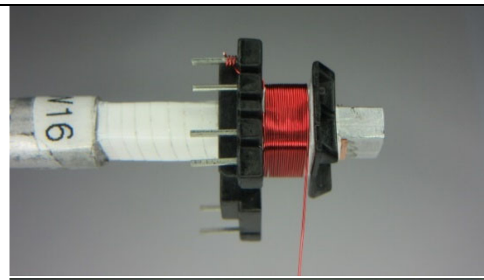
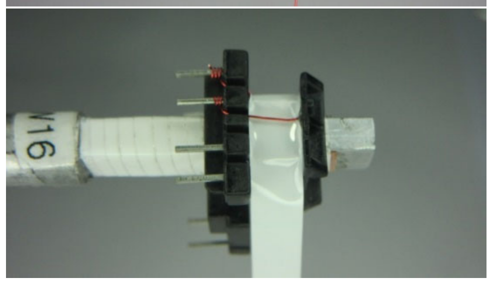
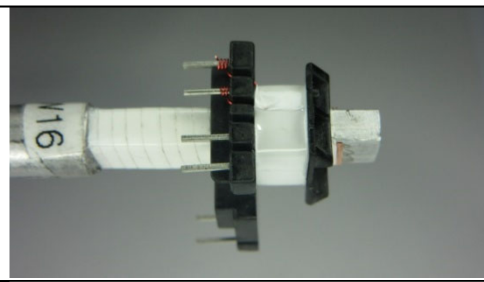
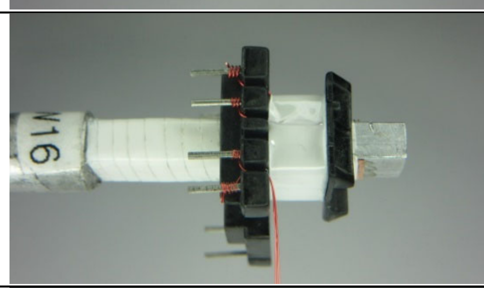
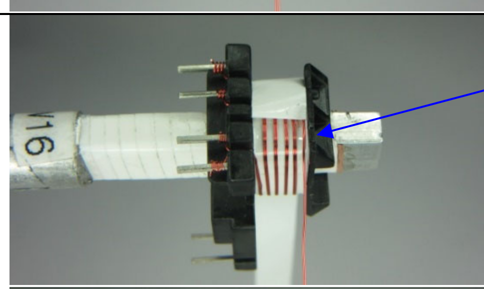
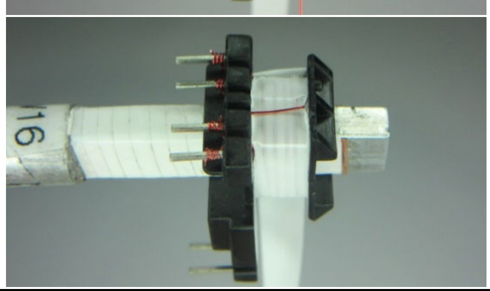
Figure 7 – Transformer Electrical Diagram.

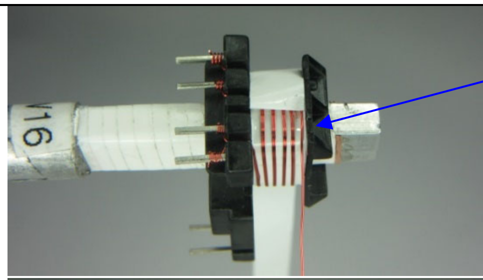
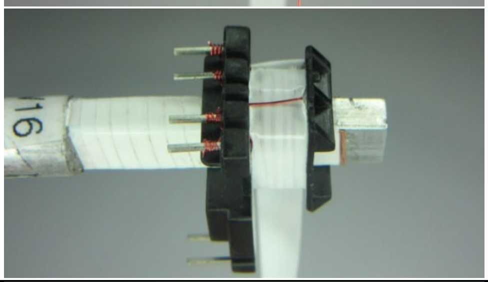
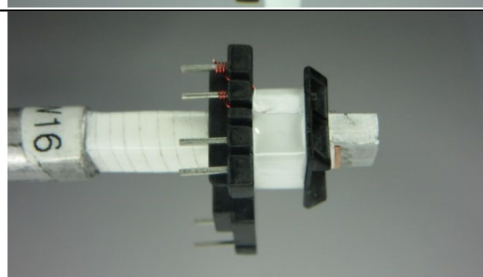
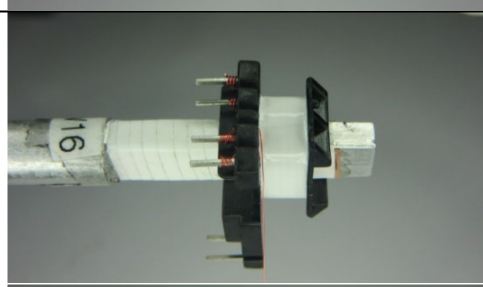
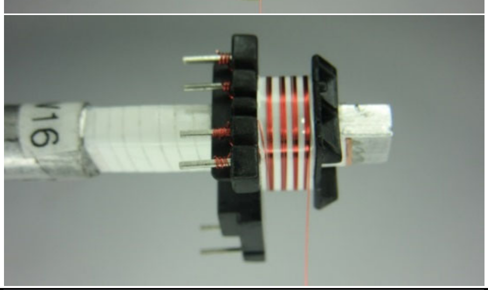
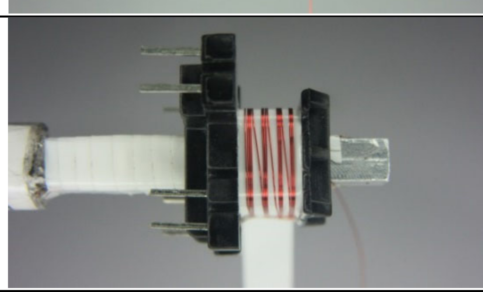
7.5 *Winding Instructions*

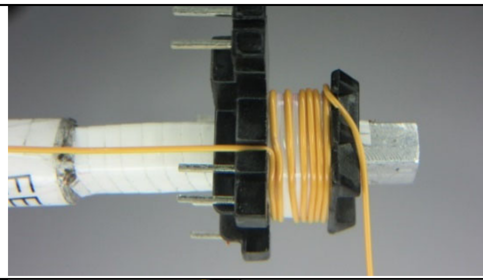
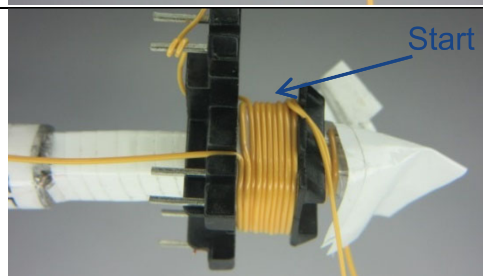
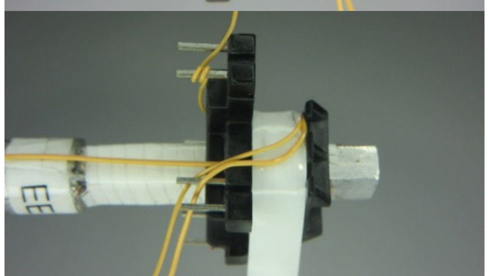
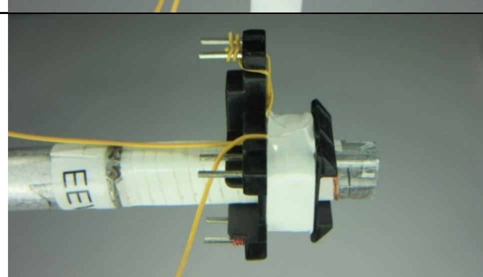
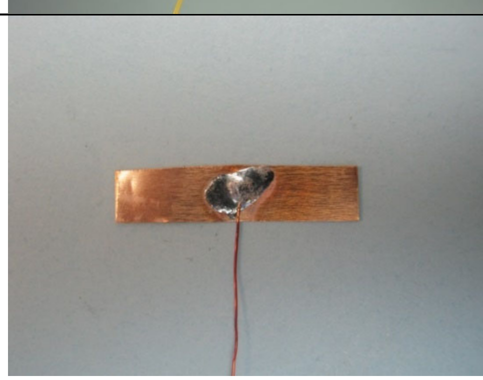
WD1 Primary	Start at pin 1, wind 23 turns of wire Item [3] from left to right and bring it back to the left and turn 2 layers of tape Item [7] for insulation. Continue to wind 23 turns on the second layer using the same wire from left to right and bring it back to the left and turn 2 layers of tape Item [7] for insulation. Continue to wind 22 turns on the third layer using the same wire from left to right and bring it back to the left and terminate the wire on pin 2.
Insulation	2 layer of tape Item [7] for insulation.
WD2A Bias & WD2B Shield	Take 3 wires Item [4], start at pin 4 for 2 wires(BIAS), start at pin 3 for 1 wire(Shield), wind 5 turns for all 3 wires from left to right, cut 1 wire (Shield)and leave no-connection for WD2B-Shield. Bring other 2 wires (Bias)to the left and terminate to pin3.
Insulation	2 layer of tape Item [7] for insulation.
WD3 Shield	Take 1 wire Item [4], start at pin 3 wind 16 turns from left to right, leave no-connection for WD3-Shield. Shield should be wind equally spaced and by 4 turns (Please see illustration).
Insulation	1 layer of tape Item [7] for insulation.
WD4A 1st Secondary & WD4B 2nd Secondary	Take 1 wire Item [5], designate start leads FL1 for WD4A. Wind 7 turns for WD4A and designate the finish lead to FL2. Take 1 wire Item [6] and start at pin6, wind first turn for WD4B beginning right after the first turn of WD4A and 2nd turn right after the 2nd turn of WD4A and 3rd turn right after the 3rd turn of WD4A. Please see illustration. Turn 1 layer of tape and bring two wire to the left and turn another 1 layer of tape for insulation. Terminate finish of WD4B to pin 5. 2 layers of tape Item [7] for secure windings and insulation
Finish	Cut short FL1 to ~22.0 mm and FL2 to ~19.0 mm. Gap the core halves to get 1180 μH. Prepare copper foil Item [8], solder wire Item [3] at the middle to connect to pin 3, and then place on top core halves. Then secure 2 core halves with 2 layers of tape Item [9]. Remove pins: 7 and 8. Varnish with Item [10].

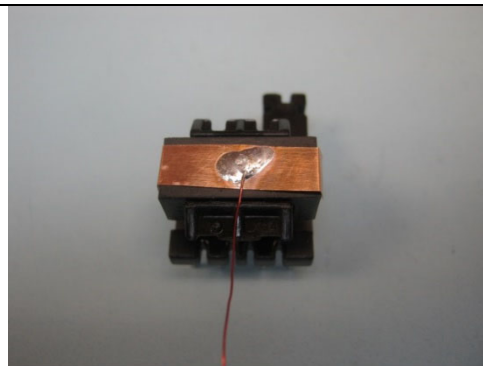
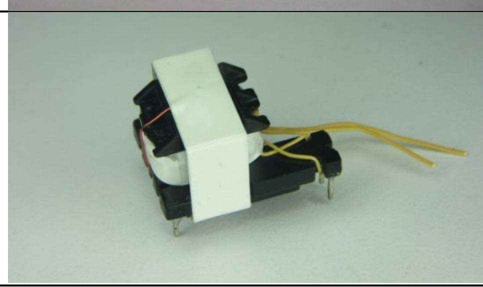
7.6 *Winding Illustrations*

		For the purpose of these instructions, bobbin Item [1] is oriented on winder such that pin side is on the left side. Winding direction is clockwise direction.
WD1 Primary (1st Layer)	  	Start at pin 1, wind 22 turns of wire Item [3] from left to right and bring it back to the left and turn 2 layers of tape Item [7] for insulation.
WD1 Primary (2nd Layer)	 	Continue to wind 22 turns on the second layer using the same wire from left to right and bring it back to the left and turn 2 layers of tape Item [7] for insulation.

WD1 Primary (3rd Layer)	 	Continue to wind 20 turns on the third layer using the same wire from left to right and bring it back to the left and terminate the wire on pin 2.
		2 layer of tape Item [7] for insulation.
		
WD2A Bias & WD2B Shield	 	Cut wire and leave no connection for WD2B Shield Bring other 2 wire (Bias)to the left and terminate to pin 3. 2 layer of tape Item [7] for insulation.

WD2A Bias & WD2B Shield	 	Cut wire and leave no connection for WD2B Shield Bring other 2 wire (Bias)to the left and terminate to pin 3. 2 layer of tape Item [7] for insulation.
		2 layer of tape Item [8] for insulation.
WD3 Shield	 	Take 1 wire Item [4], start at pin 3 wind 16 turns from left to right. Shield should be wind equally spaced and by 4 turns.
Insulation		Back View (secondary side). 1 layer of tape Item [7] for insulation.

WD4A 1st Secondary and WD4B 2nd Secondary		Take 1 wire Item [5], designate start leads FL1 for WD4A. Wind 7 turns for WD4A and designate the finish lead to FL2.
	 	Take 1 wire Item [6] and start at pin6, wind first turn for WD4B beginning right after the first turn of WD4A and 2nd turn right after the 2nd turn of WD4A and 3rd turn right after the 3rd turn of WD4A. 1 layer of tape Item [8] for insulation.
Insulation		Bring two wires to the left and turn another 1 layer of tape for insulation. Terminate finish of WD4B to pin 5.
Finish		Cut short FL1 to ~22.0 mm, and FL2 to ~19.0 mm. Gap the core halves to get 1180 μH. Prepare copper foil Item [8], solder wire Item [3] at the middle to connect to pin 3, and then place on top core halves.

	 	Then secure 2 core halves with 2 layers of tape Item [9]. Remove pins: 7 and 8. Varnish with Item [10].
Insulation		Wrap 2 layers of tape Item [9] around the transformer for insulation. Remove pins: 7 and 8. Varnish with Item [10].

8 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-EP900V_Flyback_082118; Rev.0.1; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 EP 900V Flyback Design Spreadsheet
2	APPLICATION VARIABLES					
3	VIN_MIN	90		90	V	Minimum AC input voltage
4	VIN_MAX			420	V	Maximum AC input voltage
5	VIN_RANGE			UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	22.0		22.0	uF	Input capacitor
8	VOUT	5.00		5.00	V	Output voltage at the board
9	PERCENT_CDC			0%		Percentage (of output voltage) cable drop compensation desired at full load
10	IOUT	2.000		2.000	A	Output current
11	POUT			10.00	W	Output power
12	EFFICIENCY	0.85		0.85		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
18	PRIMARY CONTROLLER SELECTION					
19	ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
20	DEVICE_GENERIC	AUTO		INN36X2		Generic device code
21	DEVICE_CODE			INN3692C		Actual device code
22	POUT_MAX			10	W	Power capability of the device based on thermal performance
23	RDSON_100DEG			11.24	Ω	Primary MOSFET on time drain resistance at 100 degC
24	ILIMIT_MIN			0.500	A	Minimum current limit of the primary MOSFET
25	ILIMIT_TYP			0.550	A	Typical current limit of the primary MOSFET
26	ILIMIT_MAX			0.600	A	Maximum current limit of the primary MOSFET
27	VDRAIN_BREAKDOWN			900	V	Device breakdown voltage
28	VDRAIN_ON_MOSFET			1.28	V	Primary MOSFET on time drain voltage
29	VDRAIN_OFF_MOSFET			777.6	V	Peak drain voltage on the primary MOSFET during turn-off
33	WORST CASE ELECTRICAL PARAMETERS					
34	FSWITCHING_MAX	81500		81500	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
35	VOR	115.0		115.0	V	Secondary voltage reflected to the primary when the primary MOSFET turns off
36	VMIN			96.52	V	Valley of the minimum input AC voltage at full load
37	KP			1.35		Measure of continuous/discontinuous mode of operation
38	MODE_OPERATION			DCM		Mode of operation
39	DUTYCYCLE			0.472		Primary MOSFET duty cycle
40	TIME_ON			7.21	us	Primary MOSFET on-time
41	TIME_OFF			6.54	us	Primary MOSFET off-time
42	LPRIMARY_MIN			1115.4	uH	Minimum primary inductance
43	LPRIMARY_TYP			1174.1	uH	Typical primary inductance
44	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
45	LPRIMARY_MAX			1232.8	uH	Maximum primary inductance

47	**PRIMARY CURRENT**					
48	IPEAK_PRIMARY			0.564	A	Primary MOSFET peak current
49	IPEDESTAL_PRIMARY			0.000	A	Primary MOSFET current pedestal
50	IAVG_PRIMARY			0.114	A	Primary MOSFET average current
51	IRIPPLE_PRIMARY			0.564	A	Primary MOSFET ripple current
52	IRMS_PRIMARY			0.207	A	Primary MOSFET RMS current
54	**SECONDARY CURRENT**					
55	IPEAK_SECONDARY			12.784	A	Secondary winding peak current
56	IPEDESTAL_SECONDARY			0.000	A	Secondary winding current pedestal
57	IRMS_SECONDARY			4.276	A	Secondary winding RMS current
61	**TRANSFORMER CONSTRUCTION PARAMETERS**					
62	**CORE SELECTION**					
63	CORE	CUSTOM	Info	CUSTOM		The transformer windings may not fit: pick a bigger core or bobbin and refer to the Transformer Parameters tab for fit calculations
64	CORE CODE	EE1621		EE1621		Core code
65	AE	32.50		32.50	mm^2	Core cross sectional area
66	LE	39.30		39.30	mm	Core magnetic path length
67	AL	2800		2800	nH/turns^2	Ungapped core effective inductance
68	VE	980.0		980.0	mm^3	Core volume
69	BOBBIN	EE1621		EE1621		Bobbin
70	AW	12.33		12.33	mm^2	Window area of the bobbin
71	BW	5.40		5.40	mm	Bobbin width
72	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
74	**PRIMARY WINDING**					
75	NPRIMARY			68		Primary turns
76	BPEAK			3426	Gauss	Peak flux density
77	BMAX			3106	Gauss	Maximum flux density
78	BAC			1553	Gauss	AC flux density (0.5 x Peak to Peak)
79	ALG			254	nH/turns^2	Typical gapped core effective inductance
80	LG			0.146	mm	Core gap length
81	LAYERS_PRIMARY			3		Number of primary layers
82	AWG_PRIMARY			33	AWG	Primary winding wire AWG
83	OD_PRIMARY_INSULATED			0.219	mm	Primary winding wire outer diameter with insulation
84	OD_PRIMARY_BARE			0.180	mm	Primary winding wire outer diameter without insulation
85	CMA_PRIMARY			242	Cmil/A	Primary winding wire CMA
87	**SECONDARY WINDING**					
88	NSECONDARY	3		3		Secondary turns
89	AWG_SECONDARY			20	AWG	Secondary winding wire AWG
90	OD_SECONDARY_INSULATED			1.118	mm	Secondary winding wire outer diameter with insulation
91	OD_SECONDARY_BARE			0.812	mm	Secondary winding wire outer diameter without insulation
92	CMA_SECONDARY			239	Cmil/A	Secondary winding wire CMA
94	**BIAS WINDING**					
95	NBIAS			8		Bias turns
99	**PRIMARY COMPONENTS SELECTION**					
100	**Line overvoltage**					
101	VOLTAGE_LINEOVREQ			428.4	V	Required AC RMS line voltage over-voltage threshold
102	RLS			5.22	MΩ	Connect two 2.61 MOhm resistors to the V-pin for the required over-voltage threshold
103	VOLTAGE_LINEOVACT			436.0	V	Actual AC RMS line over-voltage threshold
104						

105	Bias diode					
106	VBIAS			12.0	V	Rectified bias voltage
107	VF_BIAS			0.70	V	Bias winding diode forward drop
108	VREVERSE_BIASDIODE			81.71	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
109	CBIAS			22	uF	Bias winding rectification capacitor
110	CBPP			4.70	uF	BPP pin capacitor
114	**SECONDARY COMPONENTS**					
115	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
116	RFB_LOWER			34.00	kΩ	Lower feedback resistor
117	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
121	**MULTIPLE OUTPUT PARAMETERS**					
122	**OUTPUT 1**					
123	VOUT1			5.00	V	Output 1 voltage
124	IOUT1	0.30		0.30	A	Output 1 current
125	POUT1			1.50	W	Output 1 power
126	IRMS_SECONDARY1			0.641	A	Root mean squared value of the secondary current for output 1
127	IRIPPLE_CAP_OUTPUT1			0.567	A	Current ripple on the secondary waveform for output 1
128	AWG_SECONDARY1			28	AWG	Wire size for output 1
129	OD_SECONDARY1_INSULATED			0.625	mm	Secondary winding wire outer diameter with insulation for output 1
130	OD_SECONDARY1_BARE			0.321	mm	Secondary winding wire outer diameter without insulation for output 1
131	CM_SECONDARY1			128	Cmils	Bare conductor effective area in circular mils for output 1
132	NSECONDARY1			3		Number of turns for output 1
133	VREVERSE_RECTIFIER1			31.14	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
134	SRFET1	AUTO		SI2318CDS		Secondary rectifier (Logic MOSFET) for output 1
135	VF_SRFET1			0.015	V	SRFET on-time drain voltage for output 1
136	VBREAKDOWN_SRFET1			40	V	SRFET breakdown voltage for output 1
137	RDSON_SRFET1			51.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
139	**OUTPUT 2**					
140	VOUT2	12.00		12.00	V	Output 2 voltage
141	IOUT2	0.700		0.700	A	Output 2 current
142	POUT2			8.40	W	Output 2 power
143	IRMS_SECONDARY2			1.496	A	Root mean squared value of the secondary current for output 2
144	IRIPPLE_CAP_OUTPUT2			1.323	A	Current ripple on the secondary waveform for output 2
145	AWG_SECONDARY2			25	AWG	Wire size for output 2
146	OD_SECONDARY2_INSULATED			0.760	mm	Secondary winding wire outer diameter with insulation for output 2
147	OD_SECONDARY2_BARE			0.455	mm	Secondary winding wire outer diameter without insulation for output 2
148	CM_SECONDARY2			299	Cmils	Bare conductor effective area in circular mils for output 2
149	NSECONDARY2			8		Number of turns for output 2
150	VREVERSE_RECTIFIER2			81.71	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 2

151	SRFET2	AUTO		AON7254		Secondary rectifier (Logic MOSFET) for output 2
152	VF_SRFET2			0.046	V	SRFET on-time drain voltage for output 2
153	VBREAKDOWN_SRFET2			150	V	SRFET breakdown voltage for output 2
154	RDSON_SRFET2			66.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 2
156	**OUTPUT 3**					
157	VOUT3			0.00	V	Output 3 voltage
158	IOUT3			0.000	A	Output 3 current
159	POUT3			0.00	W	Output 3 power
160	IRMS_SECONDARY3			0.000	A	Root mean squared value of the secondary current for output 3
161	IRIPPLE_CAP_OUTPUT3			0.000	A	Current ripple on the secondary waveform for output 3
162	AWG_SECONDARY3			0	AWG	Wire size for output 3
163	OD_SECONDARY3_INSULATED			0.000	mm	Secondary winding wire outer diameter with insulation for output 3
164	OD_SECONDARY3_BARE			0.000	mm	Secondary winding wire outer diameter without insulation for output 3
165	CM_SECONDARY3			0	Cmils	Bare conductor effective area in circular mils for output 3
166	NSECONDARY3			0		Number of turns for output 3
167	VREVERSE_RECTIFIER3			0.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 3
168	SRFET3	AUTO		NA		Secondary rectifier (Logic MOSFET) for output 3
169	VF_SRFET3			NA	V	SRFET on-time drain voltage for output 3
170	VBREAKDOWN_SRFET3			NA	V	SRFET breakdown voltage for output 3
171	RDSON_SRFET3			NA	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 3
173	PO_TOTAL			9.90	W	Total power of all outputs
174	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
178	**TOLERANCE ANALYSIS**					
179	USER_VAC	115		115	V	Input AC RMS voltage corner to be evaluated
180	USER_ILIMIT	TYP		0.550	A	Current limit corner to be evaluated
181	USER_LPRIMARY	TYP		1174.1	uH	Primary inductance corner to be evaluated
182	MODE_OPERATION			DCM		Mode of operation
183	KP			1.937		Measure of continuous/discontinuous mode of operation
184	FSWITCHING			67341	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
185	VMIN			138.64	V	Valley of the minimum input AC voltage at full load
186	DUTYCYCLE			0.301		Steady state duty cycle
187	TIME_ON			4.47	us	Primary MOSFET on-time
188	TIME_OFF			10.38	us	Primary MOSFET off-time
189	IPEAK_PRIMARY			0.525	A	Primary MOSFET peak current
190	IPEDESTAL_PRIMARY			0.000	A	Primary MOSFET current pedestal
191	IAVERAGE_PRIMARY			0.079	A	Primary MOSFET average current
192	IRIPPLE_PRIMARY			0.525	A	Primary MOSFET ripple current
193	IRMS_PRIMARY			0.166	A	Primary MOSFET RMS current

194	BPEAK			2991	Gauss	Peak flux density
195	BMAX			2787	Gauss	Maximum flux density
196	BAC			1394	Gauss	AC flux density (0.5 x Peak to Peak)

9 Performance Data

9.1 *No-Load Input Power*

9.1.1 *Without Voltage Balancing Resistors for Input Capacitors*

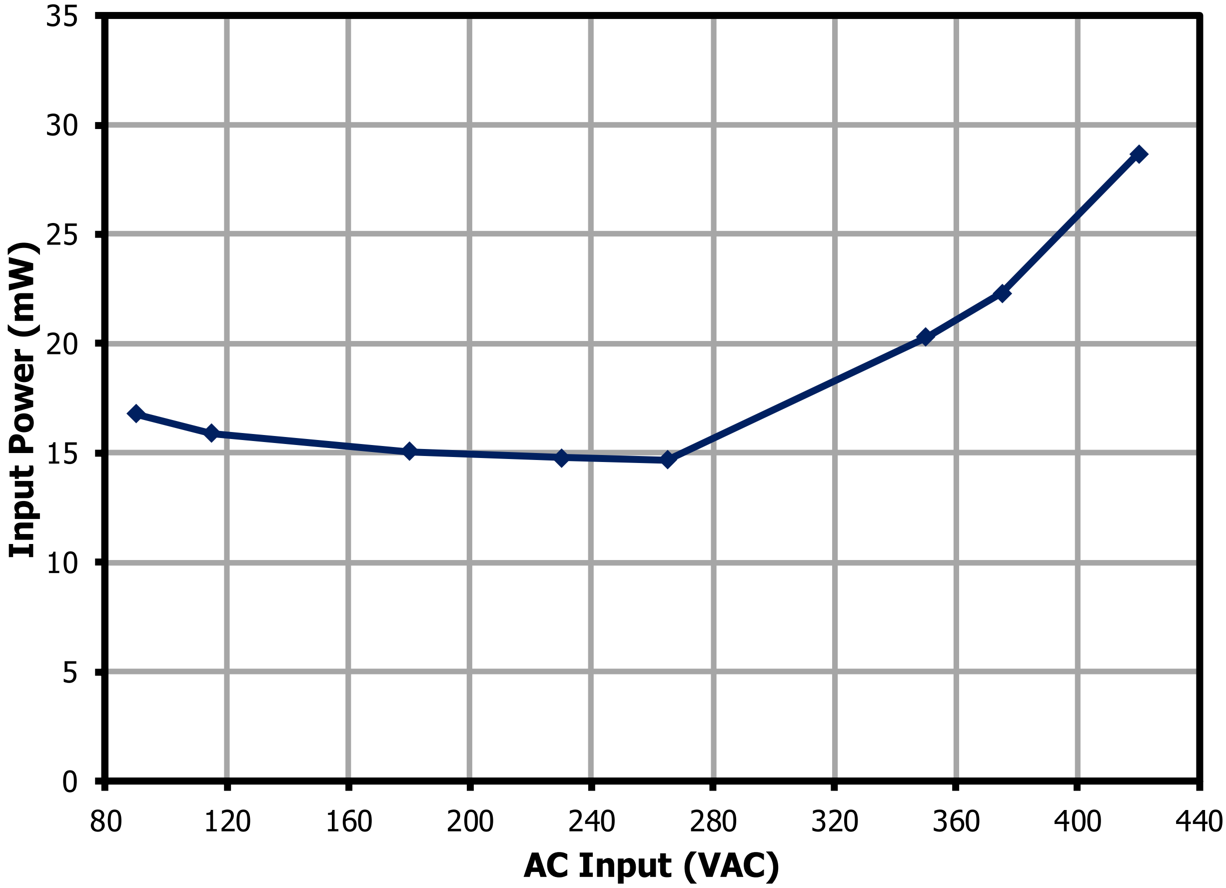


Figure 8 – No-Load Input Power vs. Line, Room Temperature.

9.1.2 *With Voltage Balancing Resistors for Input Capacitors*

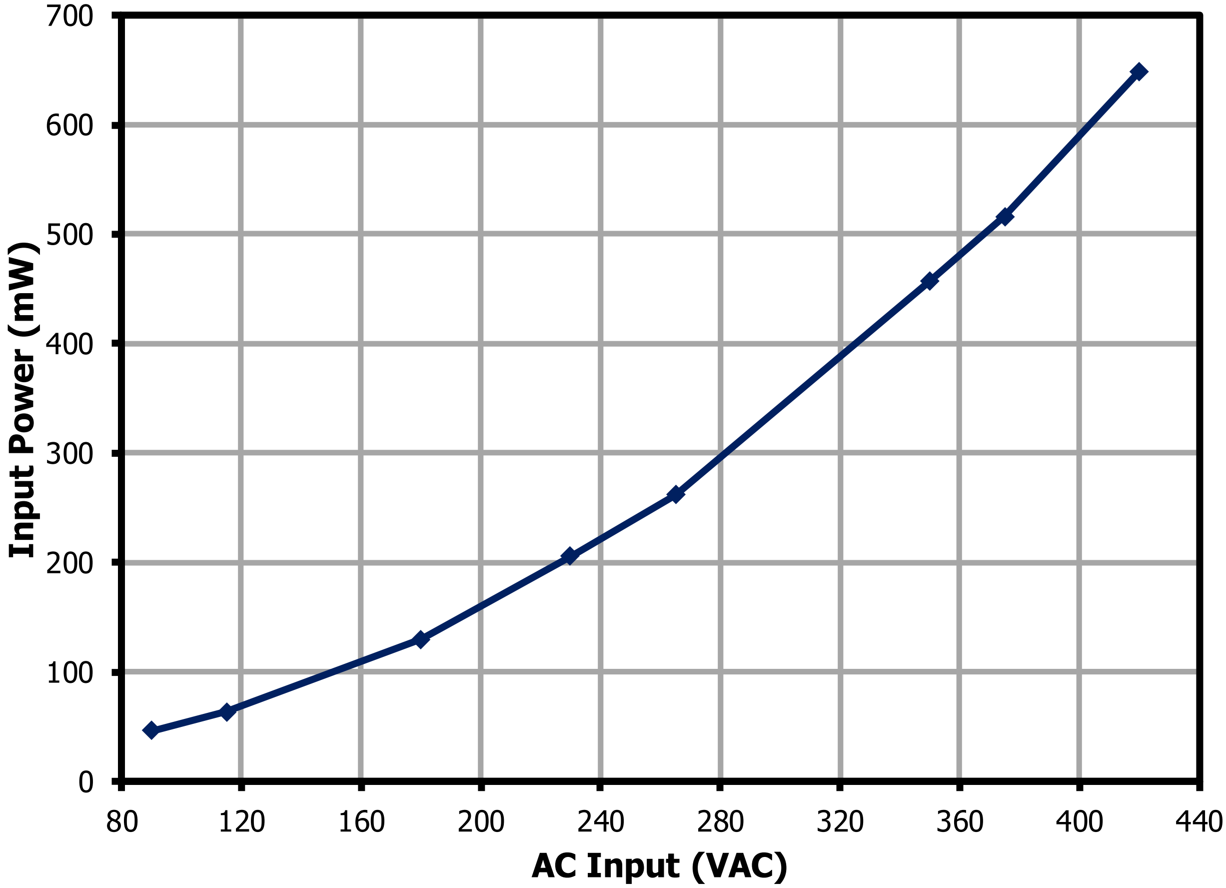


Figure 9 – No-Load Input Power vs. Line, Room Temperature.

9.2 ***Full Load Efficiency vs. Line***

9.2.1 *Without Balancing Resistors*

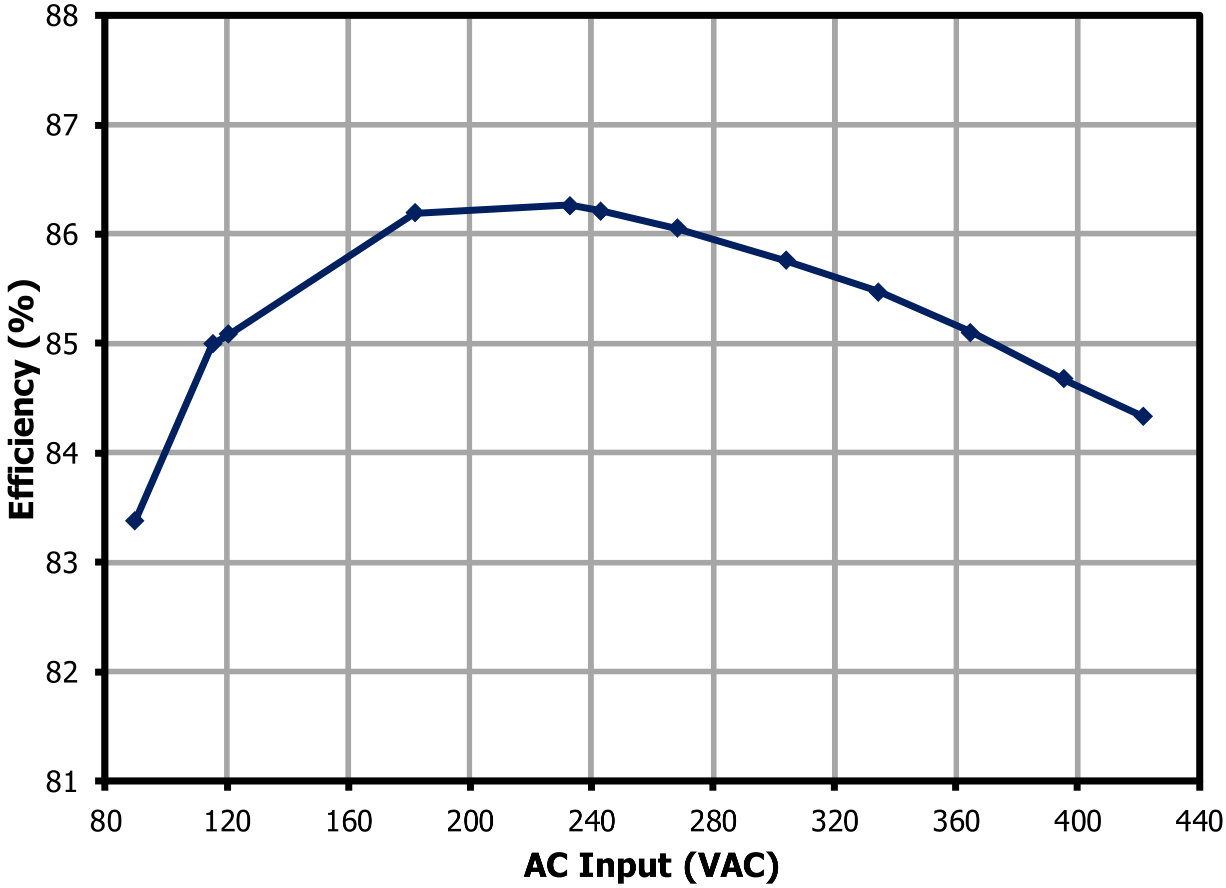


Figure 10 – Efficiency vs. Line (PCB Output Terminal), Room Temperature.

9.2.2 *With Balancing Resistors*

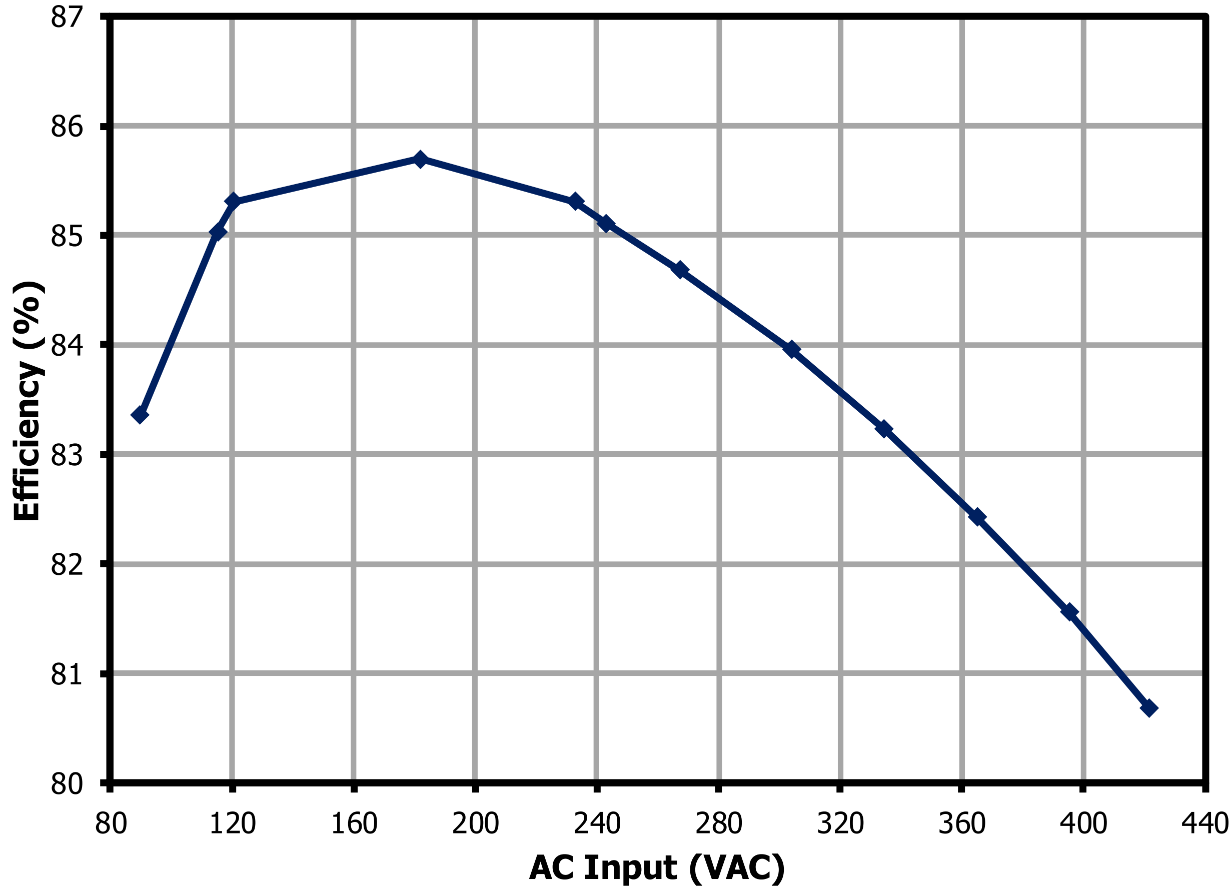


Figure 11 – Efficiency vs. Line (PCB Output Terminal), Room Temperature.

9.3 *Efficiency vs. Load*

9.3.1 *With Balancing Resistors*

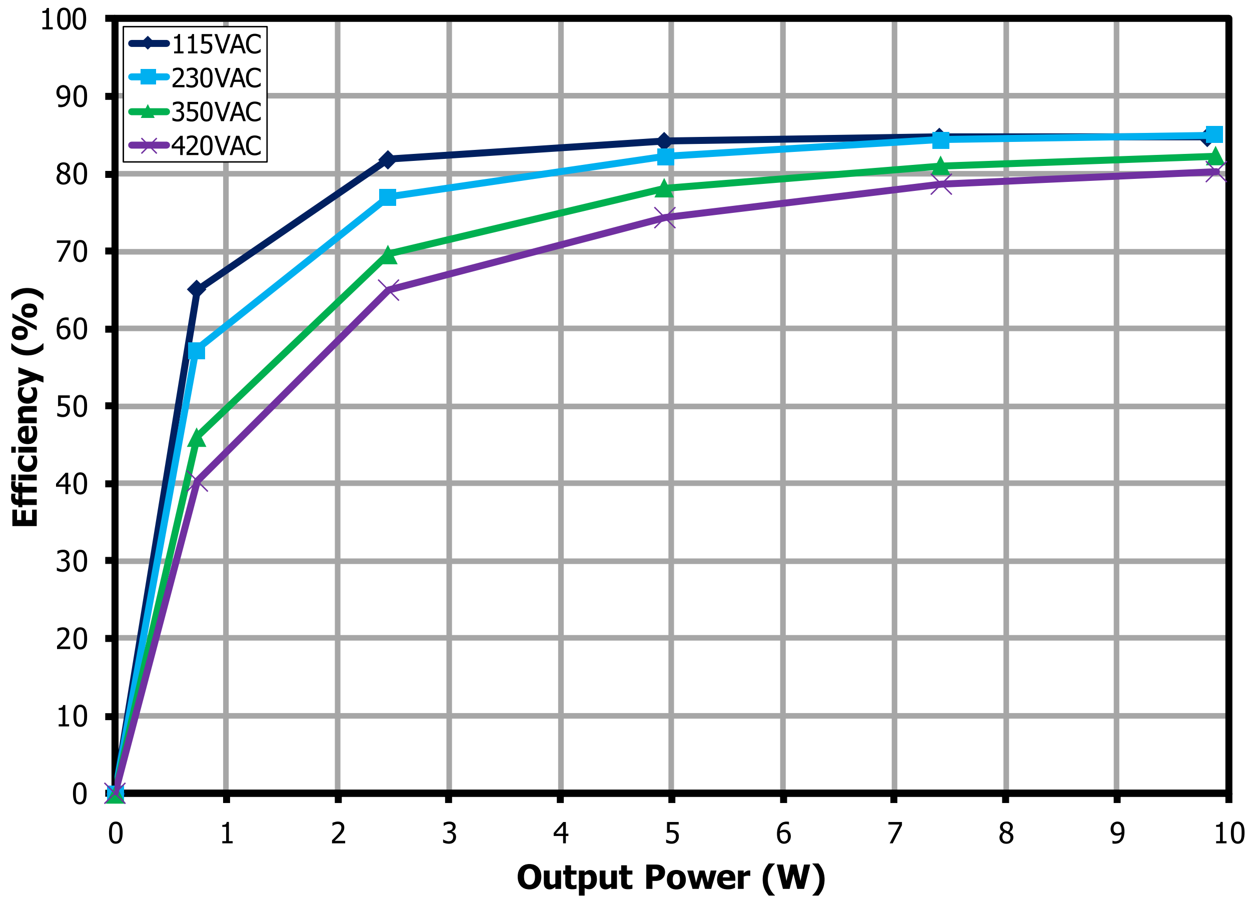


Figure 12 – Efficiency vs. Load, Room Temperature.

9.3.2 *Without Balancing Resistors*

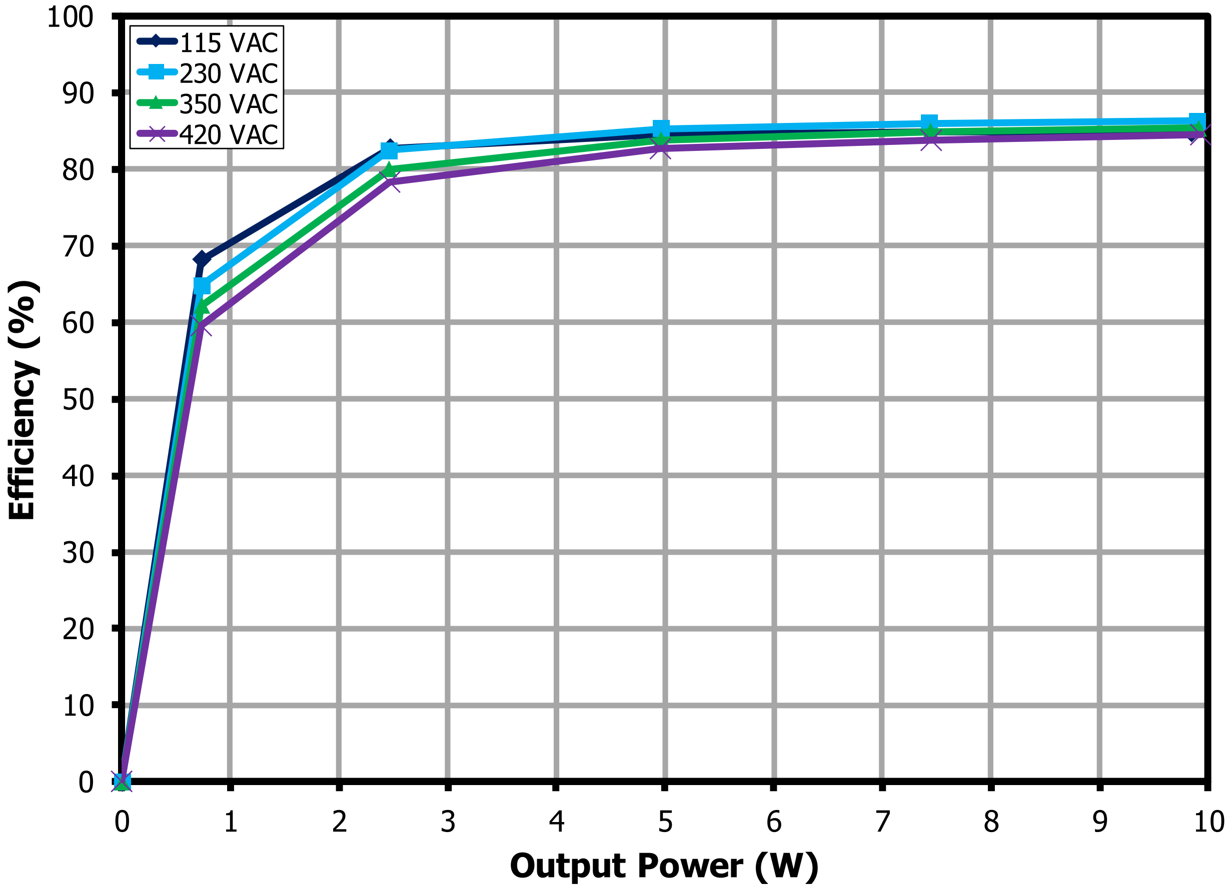


Figure 13 – Efficiency vs. Load, Room Temperature.

9.4 *Line and Load Regulation*

9.4.1 *Line Regulation (Full Load)*

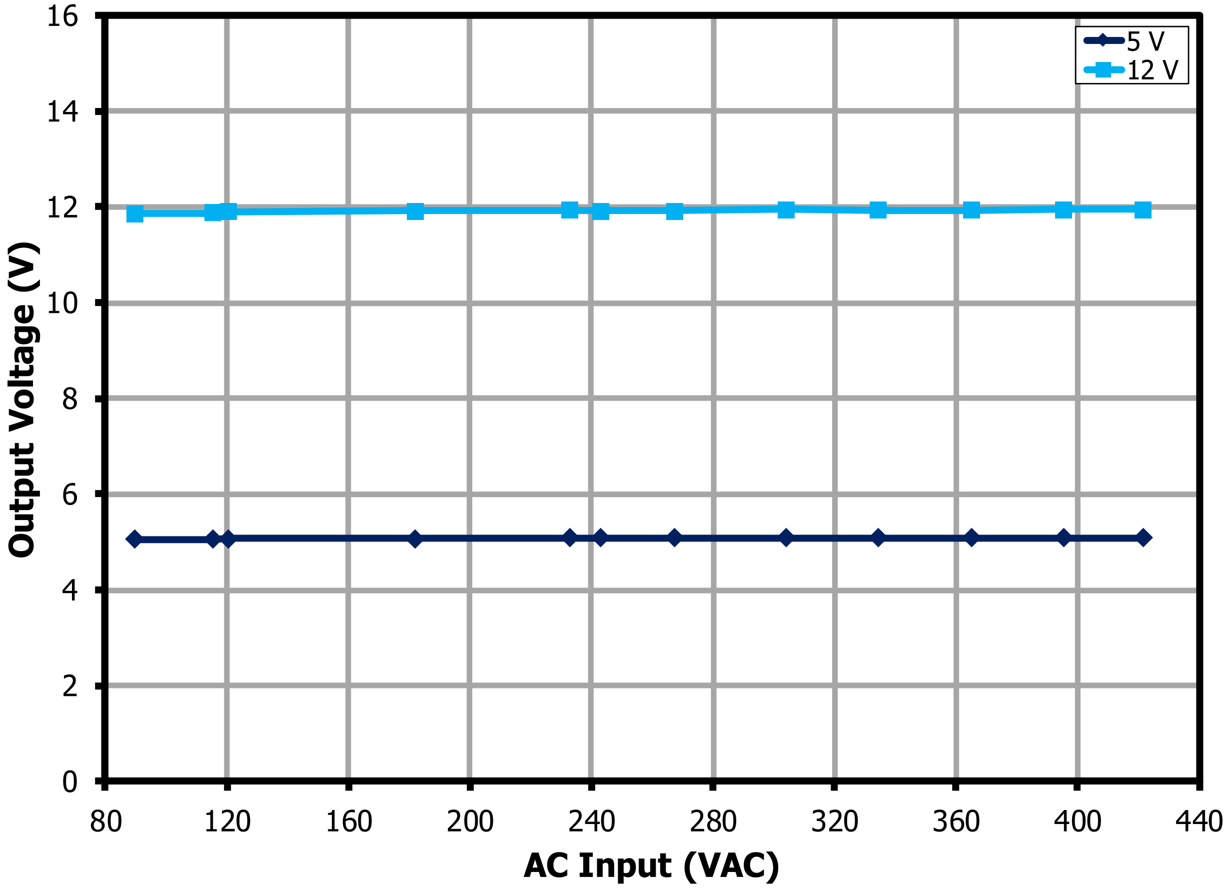


Figure 14 – Full Load Line Regulation (PCB Output Terminal), Room Temperature.

	12 V	5 V
Min	11.85	5.05
Max	11.94	5.09

9.4.2 *Cross Load Regulation*

9.4.2.1 12 V Load Change with Full Load on 5 V

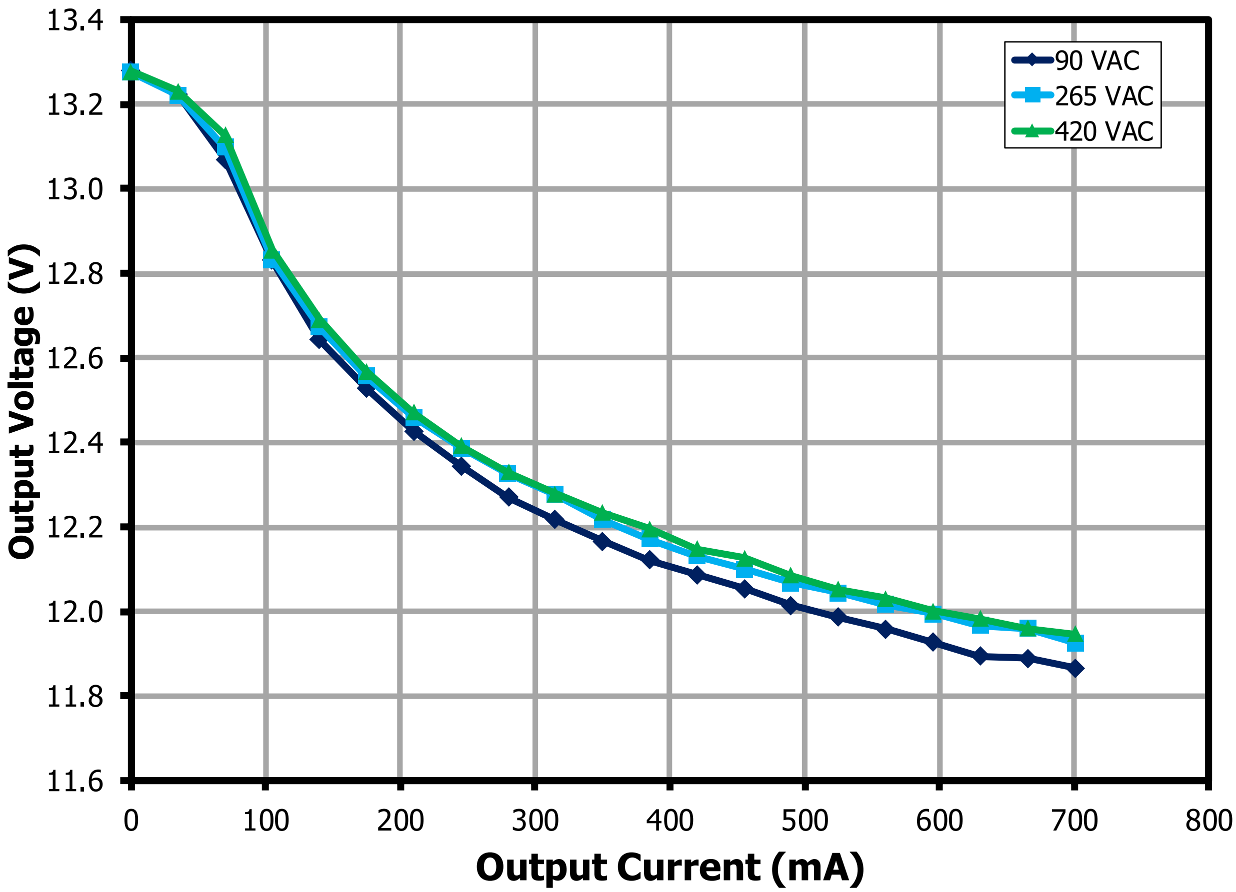


Figure 15 – Cross Regulation (PCB Output Terminal), Room Temperature.

	12 V	5 V
Min	11.87	4.94
Max	13.28	5.09

9.4.3 *12 V Load Change with No-Load on 5 V*

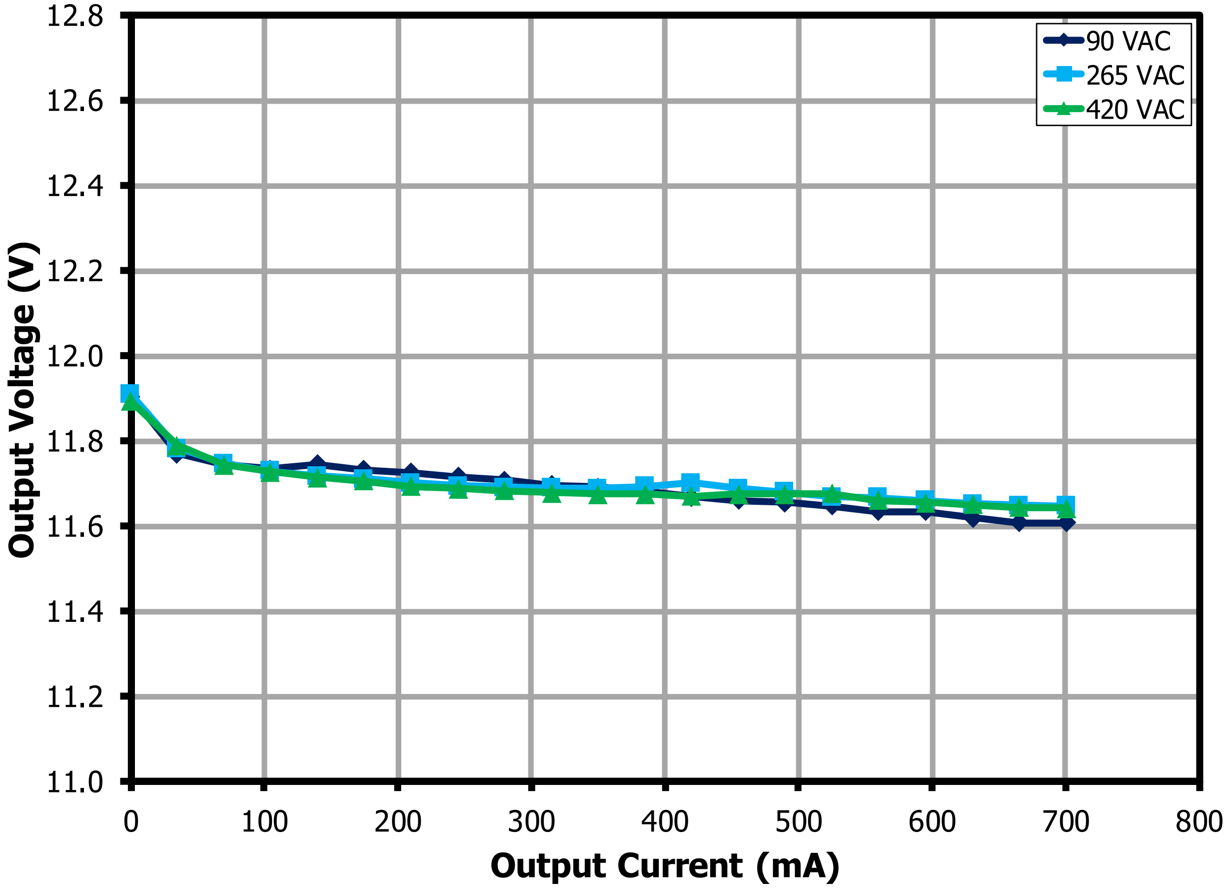


Figure 16 – Cross Regulation (PCB Output Terminal), Room Temperature.

	12 V	5 V
Min	11.61	5.11
Max	11.91	5.16

9.4.4 *5 V Load Change with Full Load on 12 V*

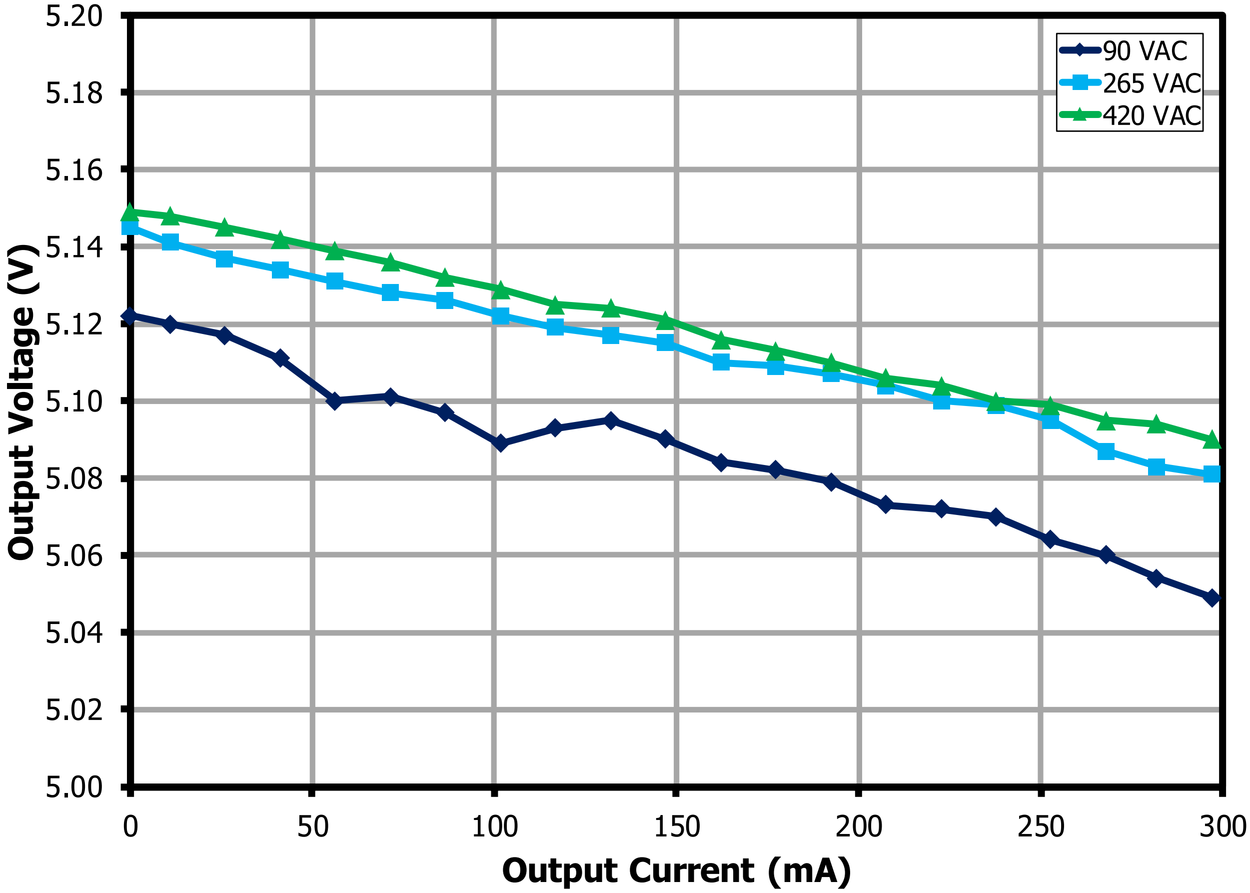


Figure 17 – Cross Regulation (PCB Output Terminal), Room Temperature.

	12 V	5 V
Min	11.58	5.05
Max	11.94	5.15

9.4.5 *5 V Load Change with No-Load on 12 V*

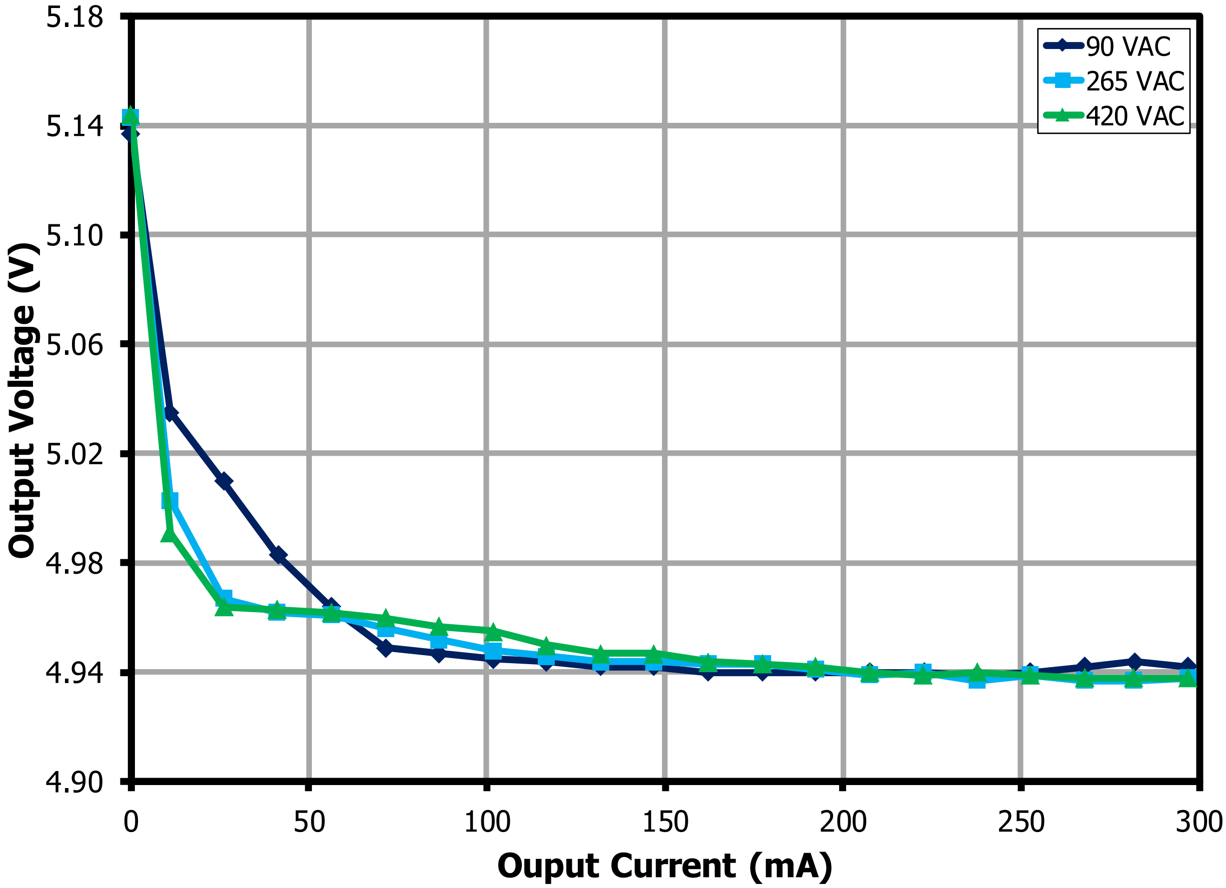


Figure 18 – Cross Regulation (PCB Output Terminal), Room Temperature.

	12 V	5 V
Min	11.90	4.94
Max	13.28	5.14

10 Thermal Performance

10.1 *90 VAC 60 Hz 100% Load*

Figure 19 – InnoSwitch3-EP Side.

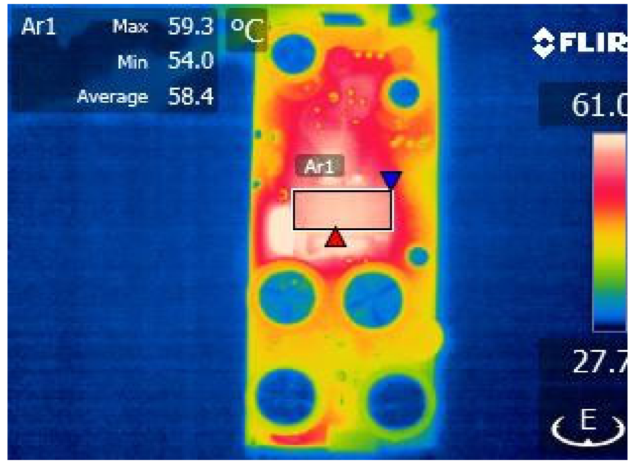


Figure 20 – Transformer Side.

V_{IN} (VAC)	Component	Temperature (°C)
90	IC (U1)	66.4
	Transformer (T1)	59.3
	Ambient	25.9

10.2 *265 VAC 50 Hz 100% Load*

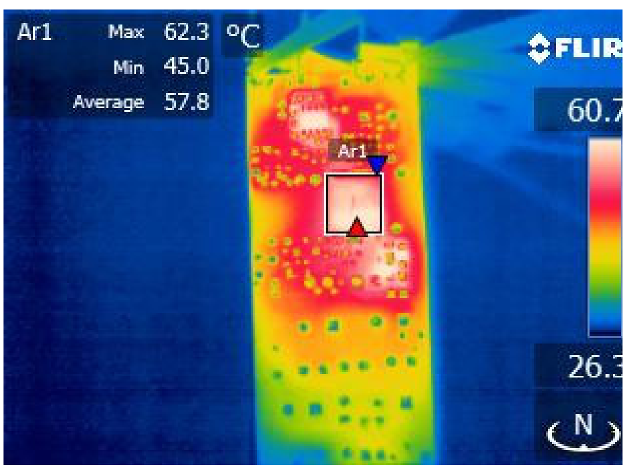


Figure 21 – InnoSwitch3-EP Side.

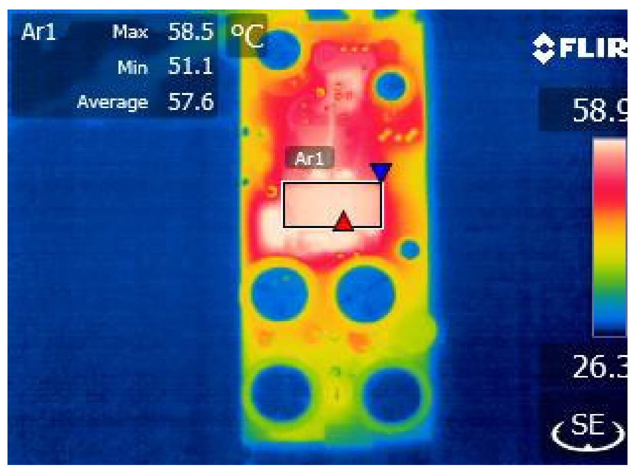


Figure 22 – Transformer Side.

V_{IN} (VAC)	Component	Temperature (°C)
265	IC (U1)	62.3
	Transformer (T1)	58.5
	Ambient	26

10.2.1 *420 VAC 50 Hz 100% Load*

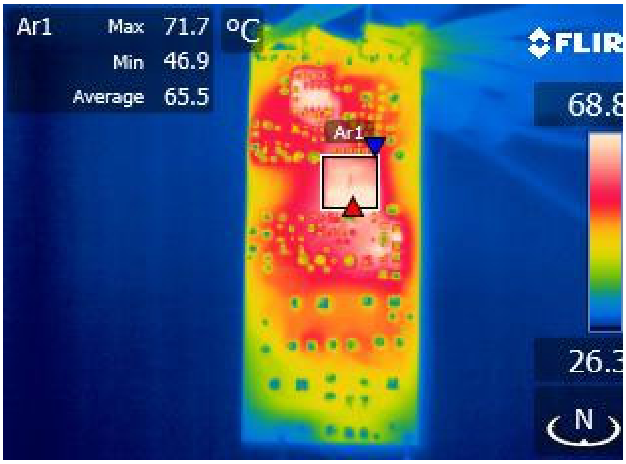


Figure 23 – InnoSwitch3-EP Side.

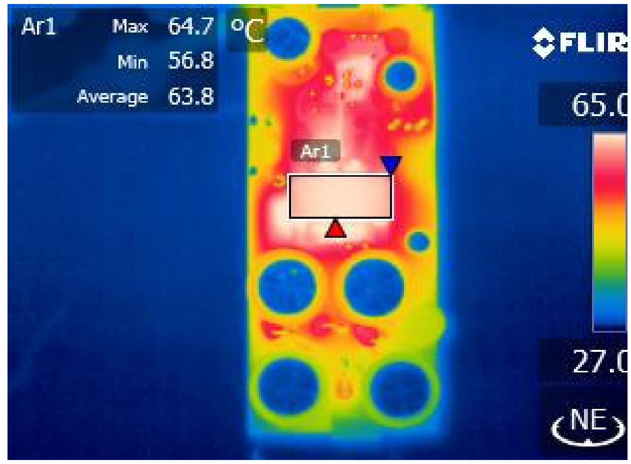


Figure 24 – Transformer Side.

V_{IN} (VAC)	Component	Temperature (°C)
420	IC (U1)	71.5
	Transformer (T1)	64.7
	Ambient	26.3

10.3 *Thermal Shutdown and Recovery*

Line (VAC)	Load (%)	Temperature		Delta (ºC)
		Shutdown (ºC)	Recovery (ºC)	
90	100	138	68	70
265	100	136	67	69
420	100	138	67	71

Figure 25 – Thermal Shutdown and Recovery.

11 Waveforms

11.1 *Drain Voltage and Current Waveforms at Normal Operation*

11.1.1 *100% Load*

Figure 26 – 90 VAC, 60 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 20 µs / div.
$V_{DS(MAX)}$: 320 V.
$I_{DS(MAX)}$: 529 mA.
Fs = 66.7 kHz.

Figure 27 – 265 VAC, 50 Hz.
CH2: V_{DS}, 200 V / div., 2 ms / div.
CH3: I_{DS}, 200 mA / div., 2 ms / div.
Zoom: 20 µs / div.
$V_{DS(MAX)}$: 568 V.
$I_{DS(MAX)}$: 549 mA.
Fs = 63.5 kHz.

Figure 28 – 420 VAC, 50 Hz.
CH2: V_{DS}, 200 V / div., 2 ms / div.
CH3: I_{DS}, 200 mA / div., 2 ms / div.
Zoom: 20 µs / div.
$V_{DS(MAX)}$: 787 V.
$I_{DS(MAX)}$: 555 mA.
Fs = 59.8 kHz.

11.1.2 *0% Load*

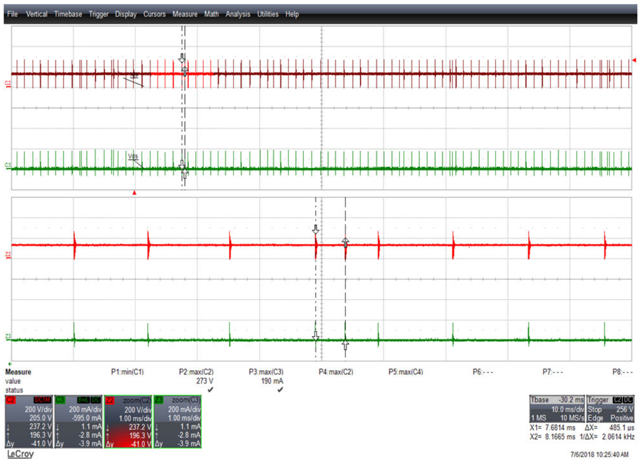


Figure 29 – 90 VAC, 60 Hz.
CH2: V_{DS}, 200 V / div., 10 ms / div.
CH3: I_{DS}, 200 mA / div., 10 ms / div.
Zoom: 1 ms / div.
$V_{DS(MAX)}$: 273 V.
$I_{DS(MAX)}$: 190 mA.
Fs = 2.0 kHz.

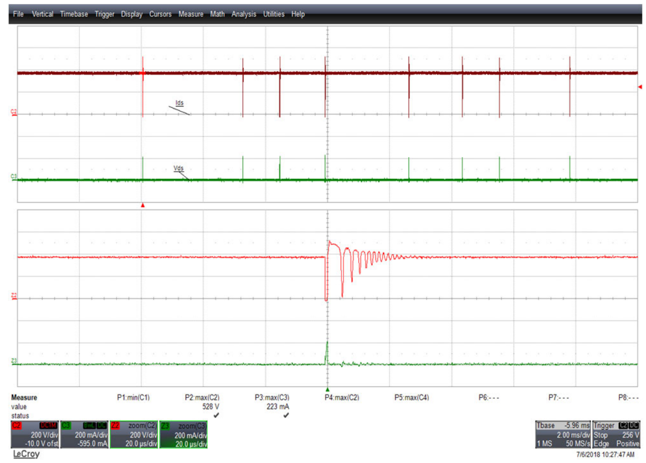


Figure 30 – 265 VAC, 50 Hz.
CH2: V_{DS}, 200 V / div., 2 ms / div.
CH3: I_{DS}, 200 mA / div., 2 ms / div.
Zoom: 1 ms / div.
$V_{DS(MAX)}$: 528 V.
$I_{DS(MAX)}$: 223 mA.

Figure 31 – 420 VAC, 50 Hz.
CH2: V_{DS}, 200 V / div., 2 ms / div.
CH3: I_{DS}, 200 mA / div., 2 ms / div.
Zoom: 100 μs / div.
$V_{DS(MAX)}$: 767 V.
$I_{DS(MAX)}$: 250 mA.

11.2 *Drain Voltage and Current at Start-Up*

11.2.1 *100% Load*

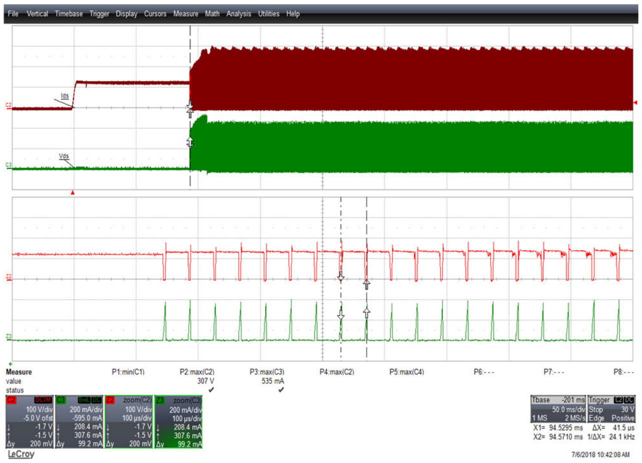


Figure 32 – 90 VAC, 60 Hz.
CH2: V_{DS}, 100 V / div., 50 ms / div.
CH3: I_{DS}, 200 mA / div., 5 ms / div.
Zoom: 100 μs / div.
$V_{DS(MAX)}$: 307 V.
$I_{DS(MAX)}$: 535 mA.
Fs = 24.1 kHz.

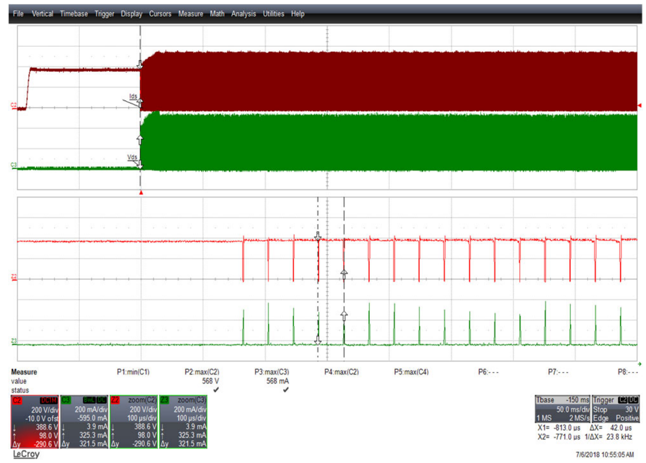


Figure 33 – 265 VAC, 50 Hz.
CH2: V_{DS}, 200 V / div., 50 ms / div.
CH3: I_{DS}, 200 mA / div., 50 ms / div.
Zoom: 100 μs / div.
$V_{DS(MAX)}$: 568 V.
$I_{DS(MAX)}$: 568 mA.
Fs = 23.8 kHz.

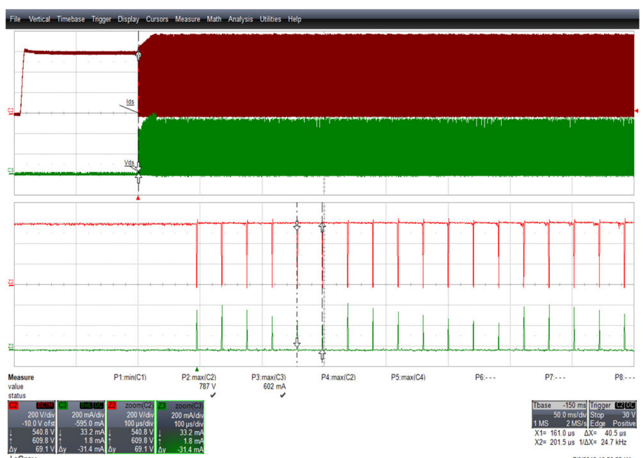


Figure 34 – 420 VAC, 50 Hz.
CH2: V_{DS}, 200 V / div., 50 ms / div.
CH3: I_{DS}, 200 mA / div., 50 ms / div.
Zoom: 100 μs / div.
$V_{DS(MAX)}$: 787 V.
$I_{DS(MAX)}$: 602 mA.
Fs = 24.7 kHz.

11.2.2 *0% Load*

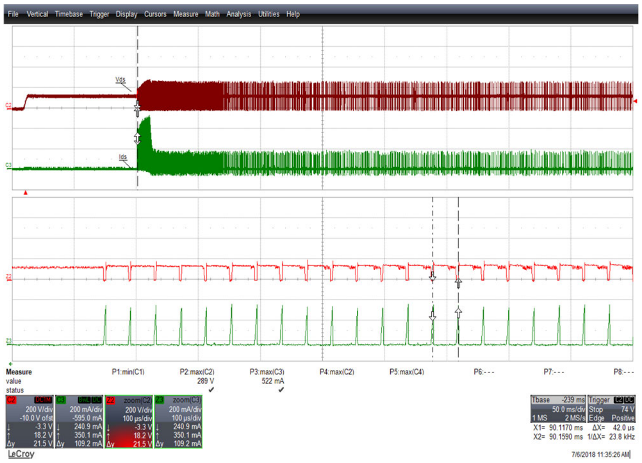


Figure 35 – 90 VAC, 60 Hz.
CH2: V_{DS}, 200 V / div., 50 ms / div.
CH3: I_{DS}, 200 mA / div., 50 ms / div.
Zoom: 100 µs / div.
$V_{DS(MAX)}$: 289 V.
$I_{DS(MAX)}$: 522 mA.
Fs = 23.8 kHz.

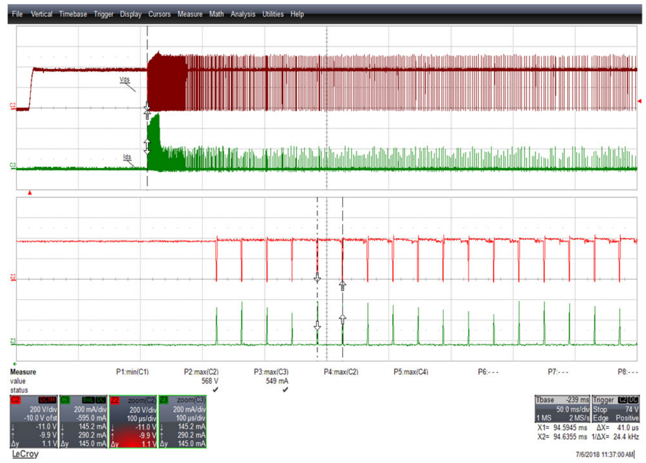


Figure 36 – 265 VAC, 50 Hz.
CH2: V_{DS}, 200 V / div., 50 ms / div.
CH3: I_{DS}, 200 mA / div., 50 ms / div.
Zoom: 100 µs / div.
$V_{DS(MAX)}$: 568 V.
$I_{DS(MAX)}$: 549 mA.
Fs = 24.4 kHz.

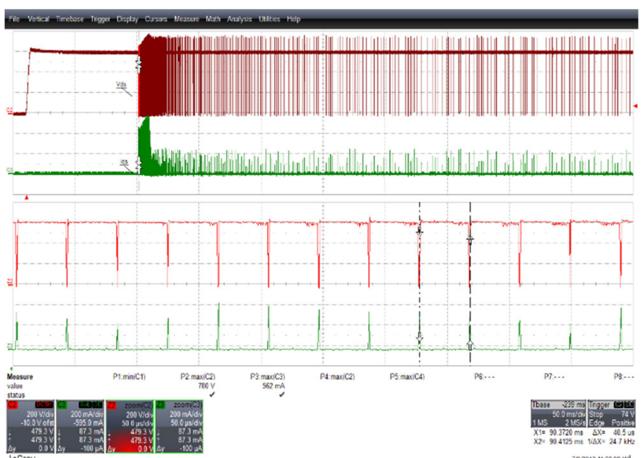


Figure 37 – 420 VAC, 50 Hz.
CH2: V_{DS}, 200 V / div., 50 ms / div.
CH3: I_{DS}, 200 mA / div., 50 ms / div.
Zoom: 50 µs / div.
$V_{DS(MAX)}$: 780 V.
$I_{DS(MAX)}$: 562 mA.
Fs = 24.7 kHz.

11.3 *Output Load Transient*

11.3.1 *12 V Output: 0%-100% (0 - 0.7 A)*

11.3.1.1 5 V Output: Full Load (0.3 A)

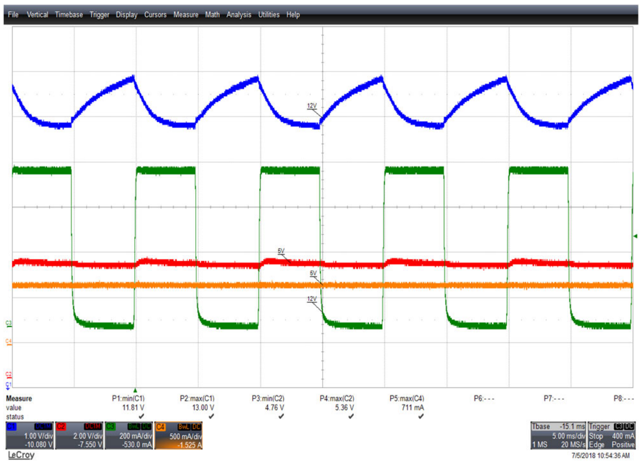


Figure 38 – Transient Response at 90 VAC, 60 Hz.
CH1: 12 V_{OUT}, 1 V / div., 5 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 5 ms / div.
CH3: 12 V_{OUT}, 200 mA / div., 5 ms / div.
CH4: 5 V_{OUT}, 500 mA / div., 5 ms / div.
12 V_{MAX}: 13 V.
12 V_{MIN}: 11.8 V.

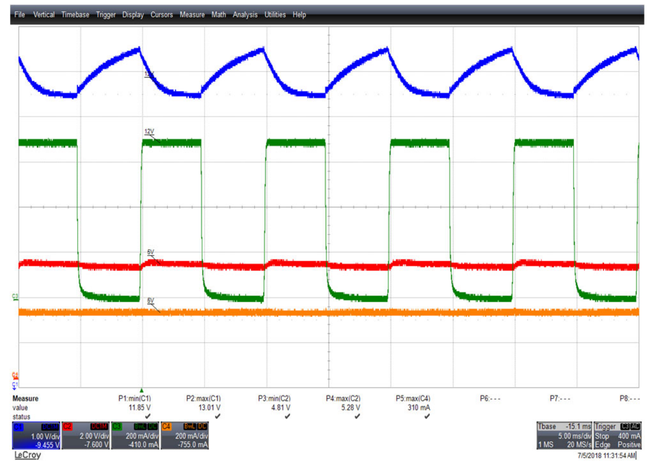


Figure 39 – Transient Response at 265 VAC, 50 Hz.
CH1: 12 V_{OUT}, 1 V / div., 5 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 5 ms / div.
CH3: 12 V_{OUT}, 200 mA / div., 5 ms / div.
CH4: 5 V_{OUT}, 200 mA / div., 5 ms / div.
12 V_{MAX}: 13 V.
12 V_{MIN}: 11.8 V.

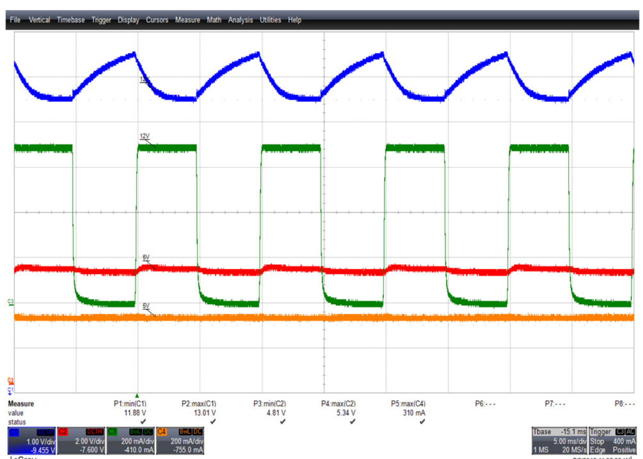


Figure 40 – Transient Response at 420 VAC, 50 Hz.
CH1: 12 V_{OUT}, 1 V / div., 5 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 5 ms / div.
CH3: 12 V_{OUT}, 200 mA / div., 5 ms / div.
CH4: 5 V_{OUT}, 200 mA / div., 5 ms / div.
12 V_{MAX}: 13 V.
12 V_{MIN}: 11.9 V.

11.3.2 *12 V Output: 50%-100% (0 - 0.7 A) Load Step*

11.3.2.1 5 V Output: Full Load (0.3 A)

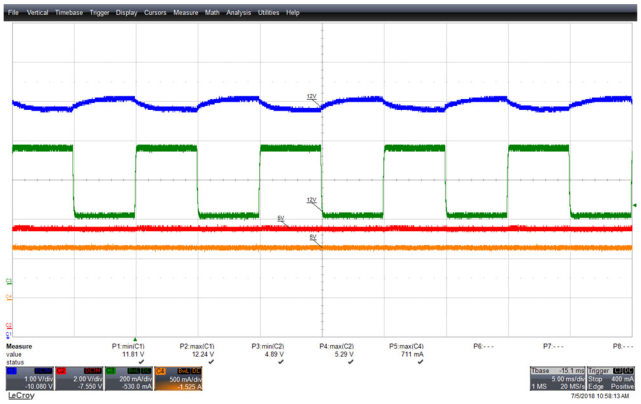


Figure 41 – Transient Response at 90 VAC, 60 Hz.
CH1: 12 V_{OUT}, 1 V / div., 5 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 5 ms / div.
CH3: 12 V_{OUT}, 200 mA / div., 5 ms / div.
CH4: 5 V_{OUT}, 500 mA / div., 5 ms / div.
12 V_{MAX}: 12.2 V.
12 V_{MIN}: 11.8 V.

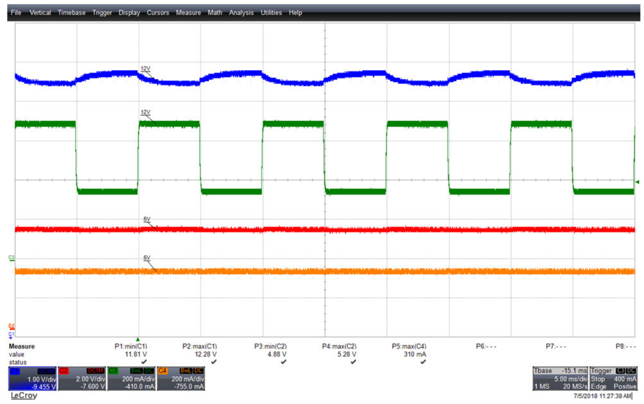


Figure 42 – Transient Response at 265 VAC, 50 Hz.
CH1: 12 V_{OUT}, 1 V / div., 5 ms / div
CH2: 5 V_{OUT}, 2 V / div., 5 ms / div.
CH3: 12 V_{OUT}, 200 mA / div., 5 ms / div
CH4: 5 V_{OUT}, 200 mA / div., 5 ms / div.
12 V_{MAX}: 12.3 V.
12 V_{MIN}: 11.8 V.

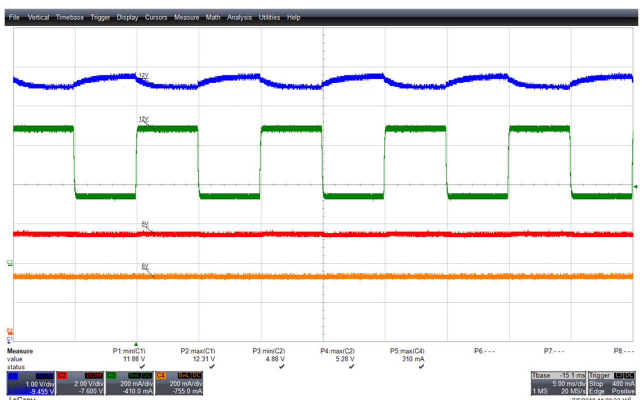


Figure 43 – Transient Response at 420 VAC, 50 Hz.
CH1: 12 V_{OUT}, 1 V / div., 5 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 5 ms / div.
CH3: 12 V_{OUT}, 200 mA / div., 5 ms / div.
CH4: 5 V_{OUT}, 200 mA / div., 5 ms / div.
12 V_{MAX}: 12.3 V.
12 V_{MIN}: 11.9 V.

11.3.3 *5 V Output: 0%-100% (0 - 0.3 A) Load Step*

11.3.3.1 12 V Output: Full Load (0.7 A)

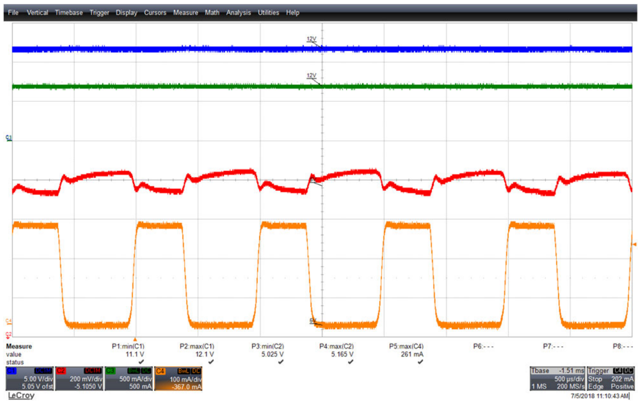


Figure 44 – Transient Response at 90 VAC, 60 Hz.
CH1: 12 V_{OUT}, 5 V / div., 500 µs / div.
CH2: 5 V_{OUT}, 200 mV / div., 500 µs / div.
CH3: 12 V_{OUT}, 500 mA / div., 500 µs / div.
CH4: 5 V_{OUT}, 100 mA / div., 500 µs / div.
5 V_{MAX}: 5.2 V.
5 V_{MIN}: 5 V.

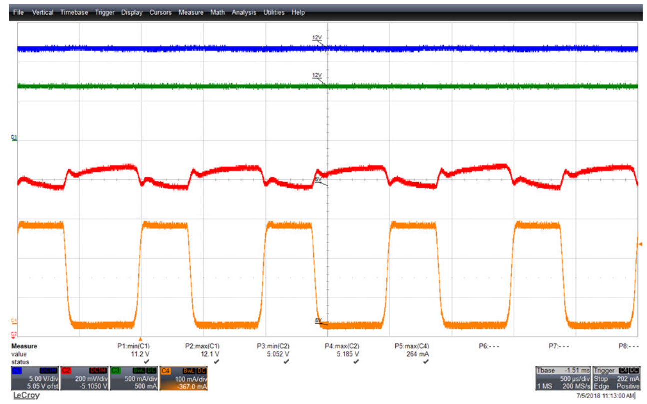


Figure 45 – Transient Response at 265 VAC, 50 Hz.
CH1: 12 V_{OUT}, 5 V / div., 500 µs / div.
CH2: 5 V_{OUT}, 200 mV / div., 500 us / div.
CH3: 12 V_{OUT}, 500 mA / div., 500 µs / div.
CH4: 5 V_{OUT}, 100 mA / div., 500 µs / div.
5 V_{MAX}: 5.2 V.
5 V_{MIN}: 5 V.

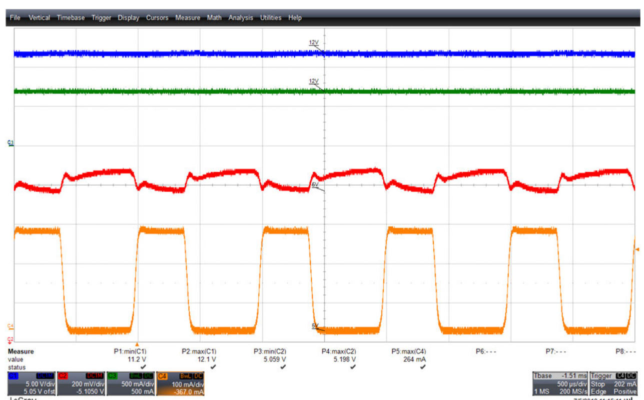


Figure 46 – Transient Response at 420 VAC, 50 Hz.
CH1: 12 V_{OUT}, 5 V / div., 500 µs / div.
CH2: 5 V_{OUT}, 200 mV / div., 500 us / div.
CH3: 12 V_{OUT}, 500 mA / div., 500 µs / div.
CH4: 5 V_{OUT}, 100 mA / div., 500 µs / div.
5 V_{MAX}: 5.2 V.
5 V_{MIN}: 5.1 V.

11.3.4 *5 V Output: 50%-100% (0.15 - 0.3 A) Load Step*

11.3.4.1 12 V Output: Full Load (0.7 A)

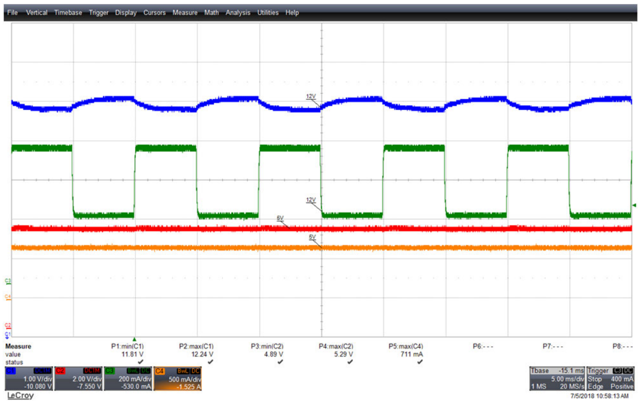


Figure 47 – Transient Response at 90 VAC, 60 Hz.
CH1: 12 V_{OUT}, 1 V / div., 5 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 5 ms / div.
CH3: 12 V_{OUT}, 200 mA / div., 5 ms / div.
CH4: 5 V_{OUT}, 500 mA / div., 5 ms / div.
5 V_{MAX}: 5.3 V.
5 V_{MIN}: 4.9 V.

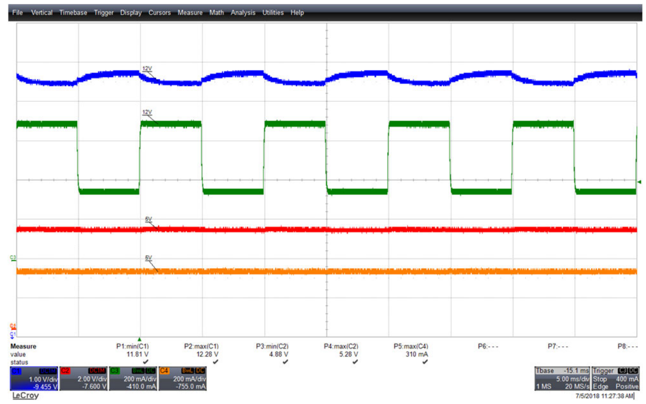


Figure 48 – Transient Response at 265 VAC, 50 Hz.
CH1: 12 V_{OUT}, 1 V / div., 5 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 5 ms / div.
CH3: 12 V_{OUT}, 200 mA / div., 5 ms / div.
CH4: 5 V_{OUT}, 500 mA / div., 5 ms / div.
5 V_{MAX}: 5.3 V.
5 V_{MIN}: 4.9 V.

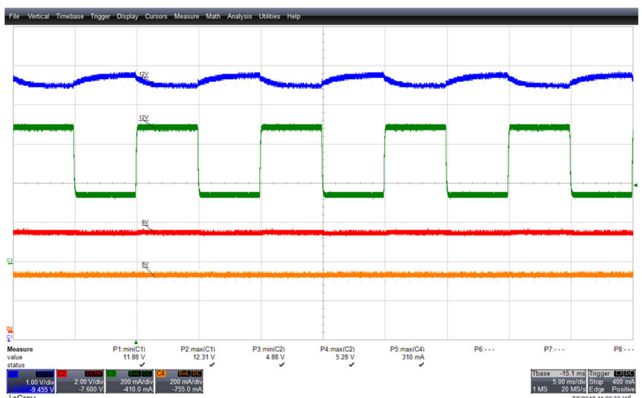


Figure 49 – Transient Response at 420 VAC, 50 Hz.
CH1: 12 V_{OUT}, 1 V / div., 5 ms / div
CH2: 5 V_{OUT}, 2 V / div., 5 ms / div.
CH3: 12 V_{OUT}, 200 mA / div., 5 ms / div
CH4: 5 V_{OUT}, 500 mA / div., 5 ms / div.
5 V_{MAX}: 5.3 V.
5 V_{MIN}: 4.9 V.

11.4 *Output Ripple Measurements*

11.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF / 50 V ceramic type and one (1) 47 μF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

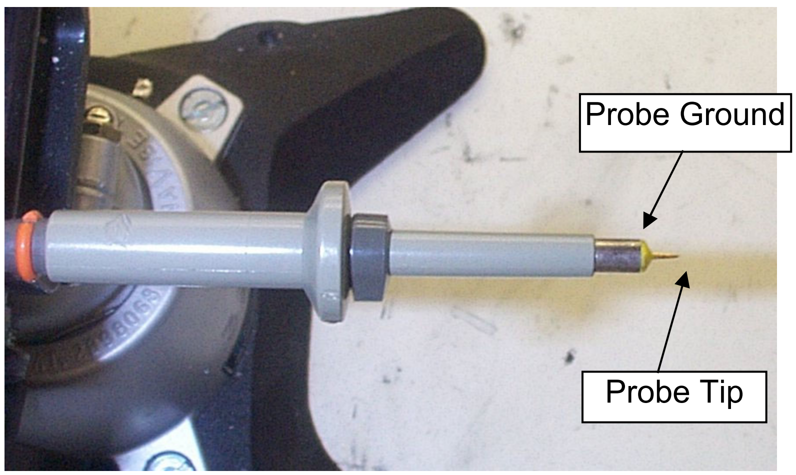


Figure 50 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

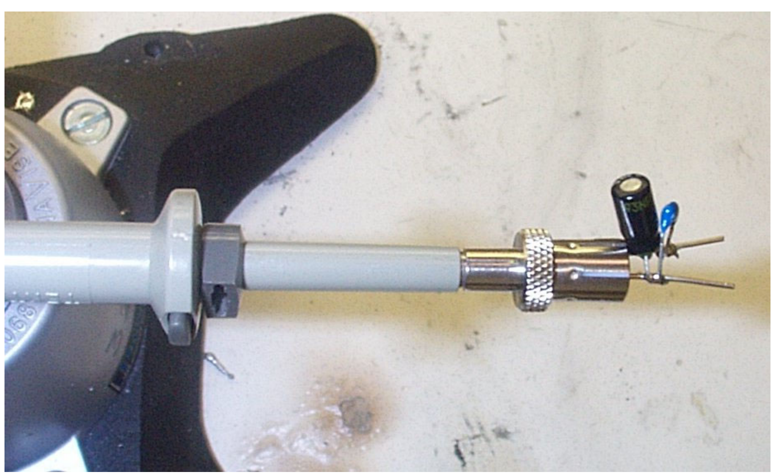


Figure 51 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

11.5 *Output Voltage Ripple*

11.5.1 *100% Load (12 V / 0.7 A, 5 V / 0.3 A)*

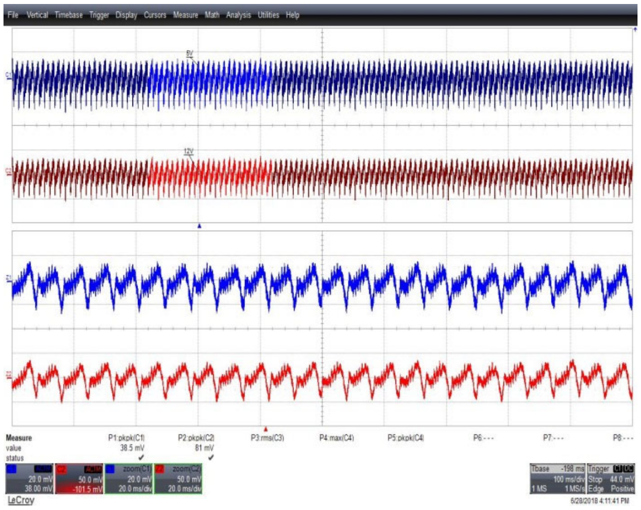


Figure 52 – 90 VAC, 60 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 20 mV / div., 100 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 50 mV / div., 100 ms, 20 ms / div.
Zoom: 20 ms / div.
Measured 5 V Ripple = 38.5 mV_{PK-PK}.
Measured 12 V Ripple = 81 mV_{PK-PK}.

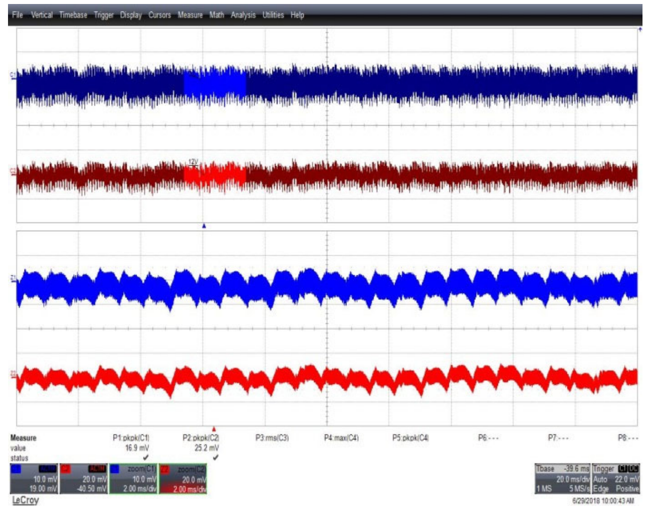


Figure 53 – 265 VAC, 50 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 20 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 20 ms, 20 ms / div.
Zoom: 2 ms / div.
Measured 5 V Ripple = 16.9 mV_{PK-PK}.
Measured 12 V Ripple = 25.2 mV_{PK-PK}.

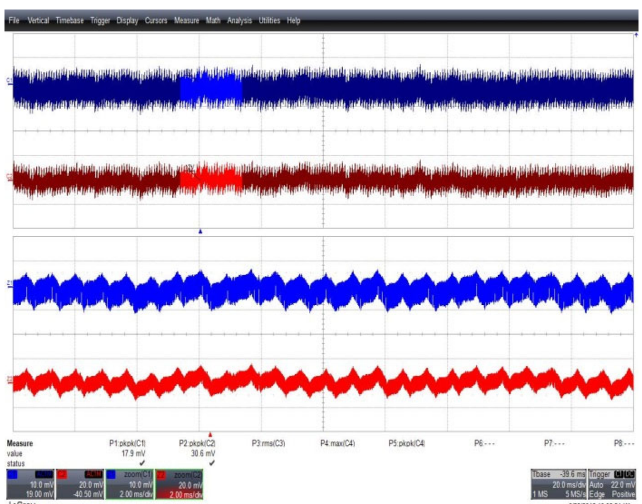


Figure 54 – 420 VAC, 50 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 20 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 20 ms, 20 ms / div.
Zoom: 2 ms / div.
Measured 5 V Ripple = 17.9 mV_{PK-PK}.
Measured 12 V Ripple = 30.6 mV_{PK-PK}.

11.5.2 *75% Load*

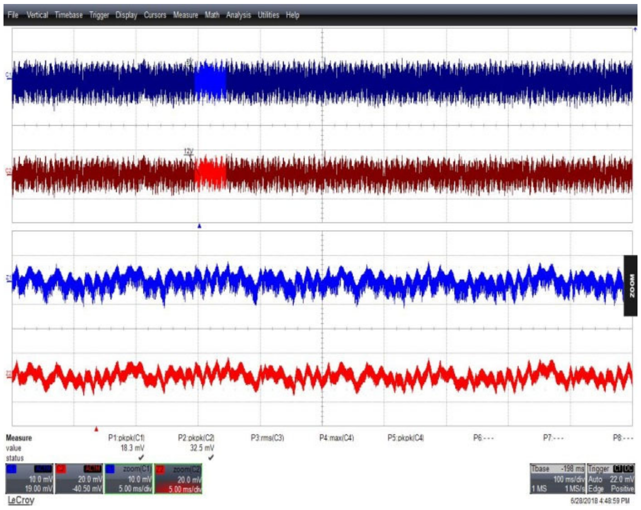


Figure 55 – 90 VAC, 60 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 100 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 100 ms, 20 ms / div.
Zoom: 5 ms / div.
Measured 12 V Ripple = 32.5 mV_{PK-PK}.
Measured 5 V Ripple = 18.3 mV_{PK-PK}.

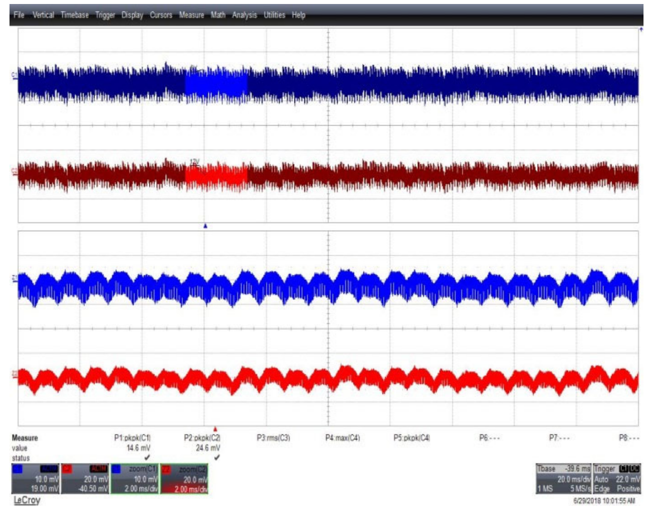


Figure 56 – 265 VAC, 50 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 20 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 20 ms / div.
Zoom: 5 ms / div.
Measured 12 V Ripple = 24.6 mV_{PK-PK}.
Measured 5 V Ripple = 14.6 mV_{PK-PK}.

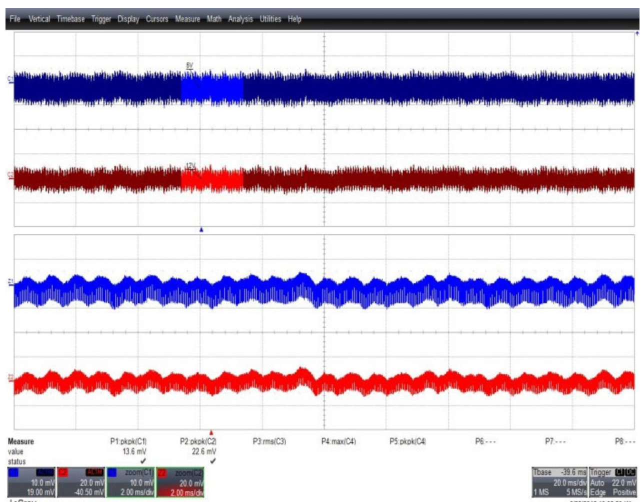


Figure 57 – 420 VAC, 50 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 20 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 20 ms / div.
Zoom: 2 ms / div.
Measured 12 V Ripple = 22.6 mV_{PK-PK}.
Measured 5 V Ripple = 13.6 mV_{PK-PK}.

11.5.3 *50% Load*

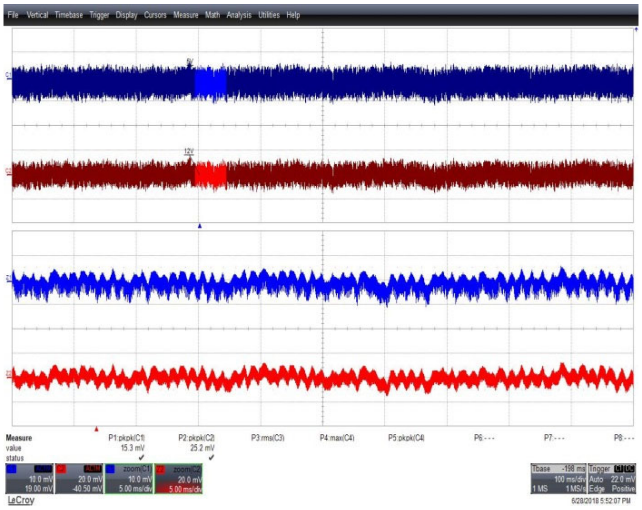


Figure 58 – 90 VAC, 60 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 100 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 100 ms / div.
Zoom: 5 ms / div.
Measured 12 V Ripple = 25.2 mV_{PK-PK}.
Measured 5 V Ripple = 15.3 mV_{PK-PK}.

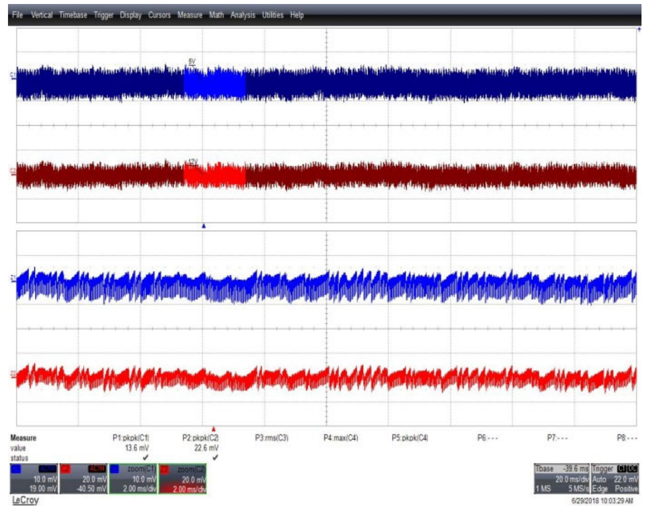


Figure 59 – 265 VAC, 50 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 20 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 20 ms / div.
Zoom: 5 ms / div.
Measured 12 V Ripple = 22.6 mV_{PK-PK}.
Measured 5 V Ripple = 13.6 mV_{PK-PK}.

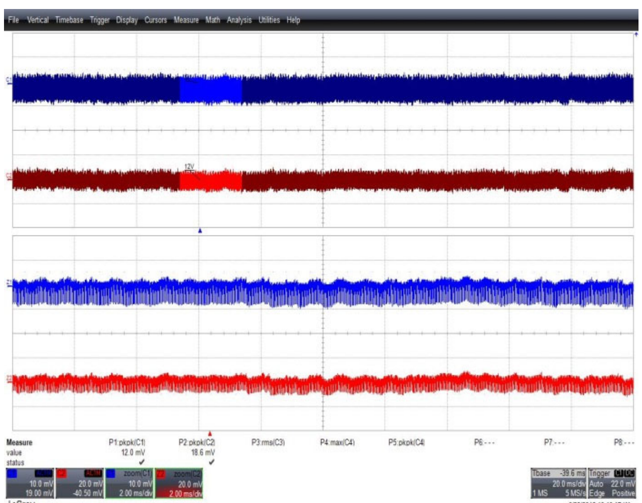


Figure 60 – 420 VAC, 50 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 20 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 20 ms / div.
Zoom: 2 ms / div.
Measured 12 V Ripple = 18.6 mV_{PK-PK}.
Measured 5 V Ripple = 12 mV_{PK-PK}.

11.5.4 *25% Load*

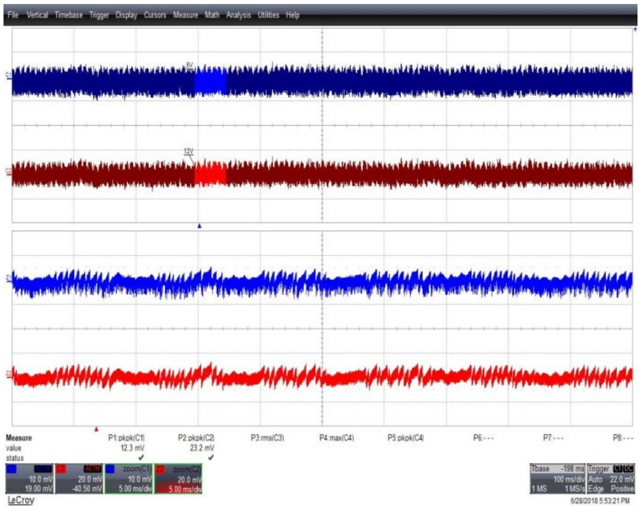


Figure 61 – 90 VAC, 60 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 100 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 100 ms / div.
Zoom: 5 ms / div.
Measured 12 V Ripple = 23.2 mV_{PK-PK}.
Measured 5 V Ripple = 12.3 mV_{PK-PK}.

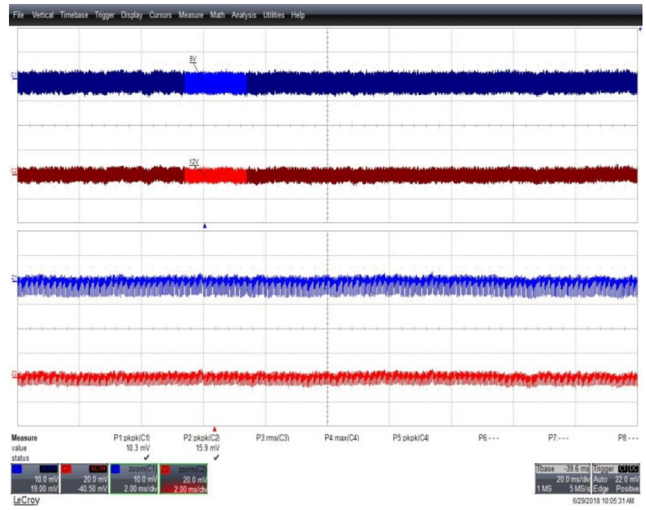


Figure 62 – 265 VAC, 50 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 20 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 20 ms / div.
Zoom: 5 ms / div.
Measured 12 V Ripple = 15.9 mV_{PK-PK}.
Measured 5 V Ripple = 10.3 mV_{PK-PK}.

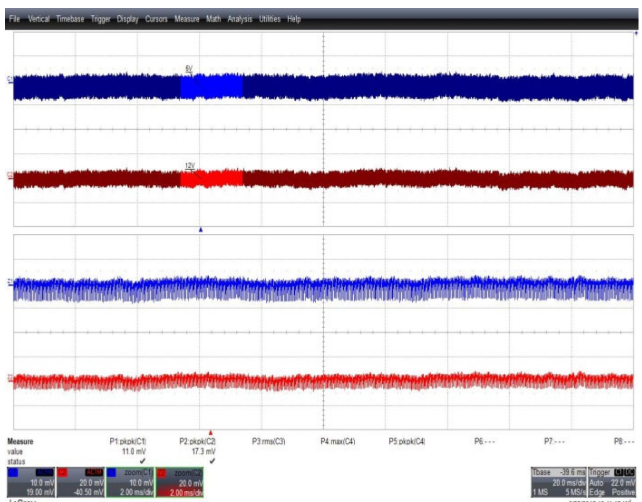


Figure 63 – 420 VAC, 50 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 20 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 20 ms / div.
Zoom: 2 ms / div.
Measured 12 V Ripple = 17.3 mV_{PK-PK}.
Measured 5 V Ripple = 11 mV_{PK-PK}.

11.5.5 *0% Load*

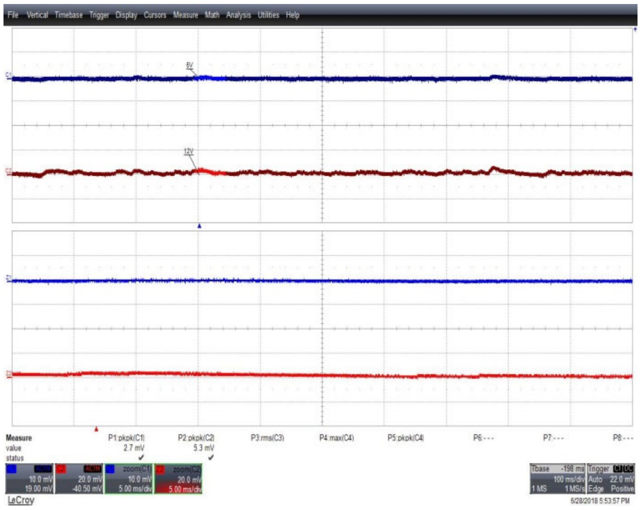


Figure 64 – 90 VAC, 60 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 100 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 100 ms / div.
Zoom: 2 ms / div.
Measured 12 V Ripple = 5.3 mV_{PK-PK}.
Measured 5 V Ripple = 2.7 mV_{PK-PK}.

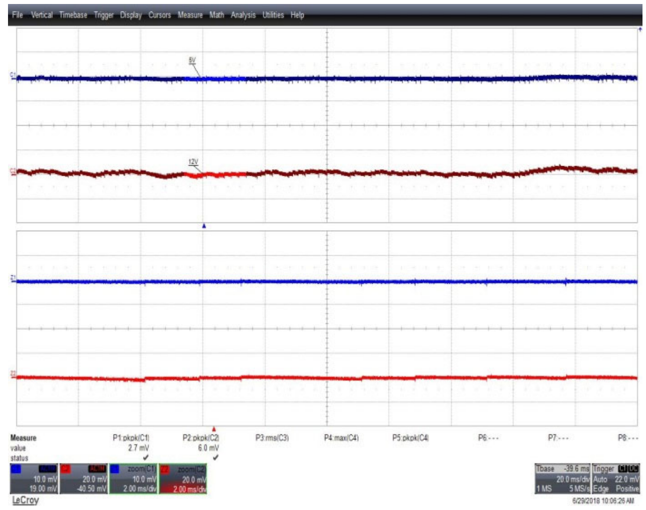


Figure 65 – 265 VAC, 60 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 20 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 20 ms / div.
Zoom: 2 ms / div.
Measured 12 V Ripple = 6 mV_{PK-PK}.
Measured 5 V Ripple = 2.7 mV_{PK-PK}.

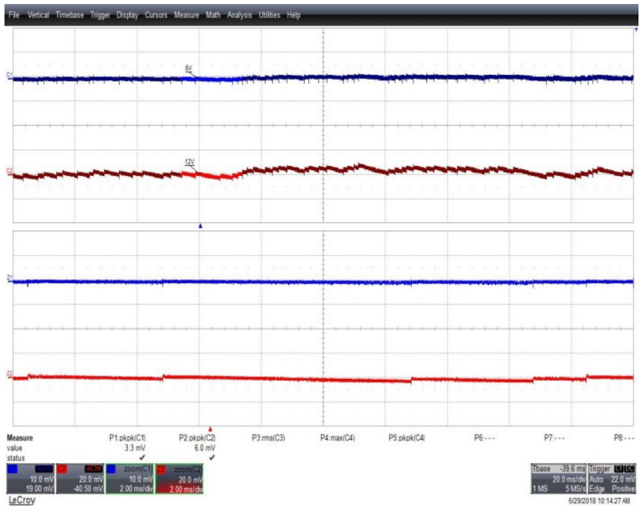


Figure 66 – 420 VAC, 50 Hz.
Ch1: 5 $V_{OUTRIPPLE}$, 10 mV / div., 20 ms / div.
Ch2: 12 $V_{OUTRIPPLE}$, 20 mV / div., 20 ms / div.
Zoom: 2 ms / div.
Measured 12 V Ripple = 6 mV_{PK-PK}.
Measured 5 V Ripple = 3.3 mV_{PK-PK}.

11.5.6 *Summary of Output Ripple vs. Load*

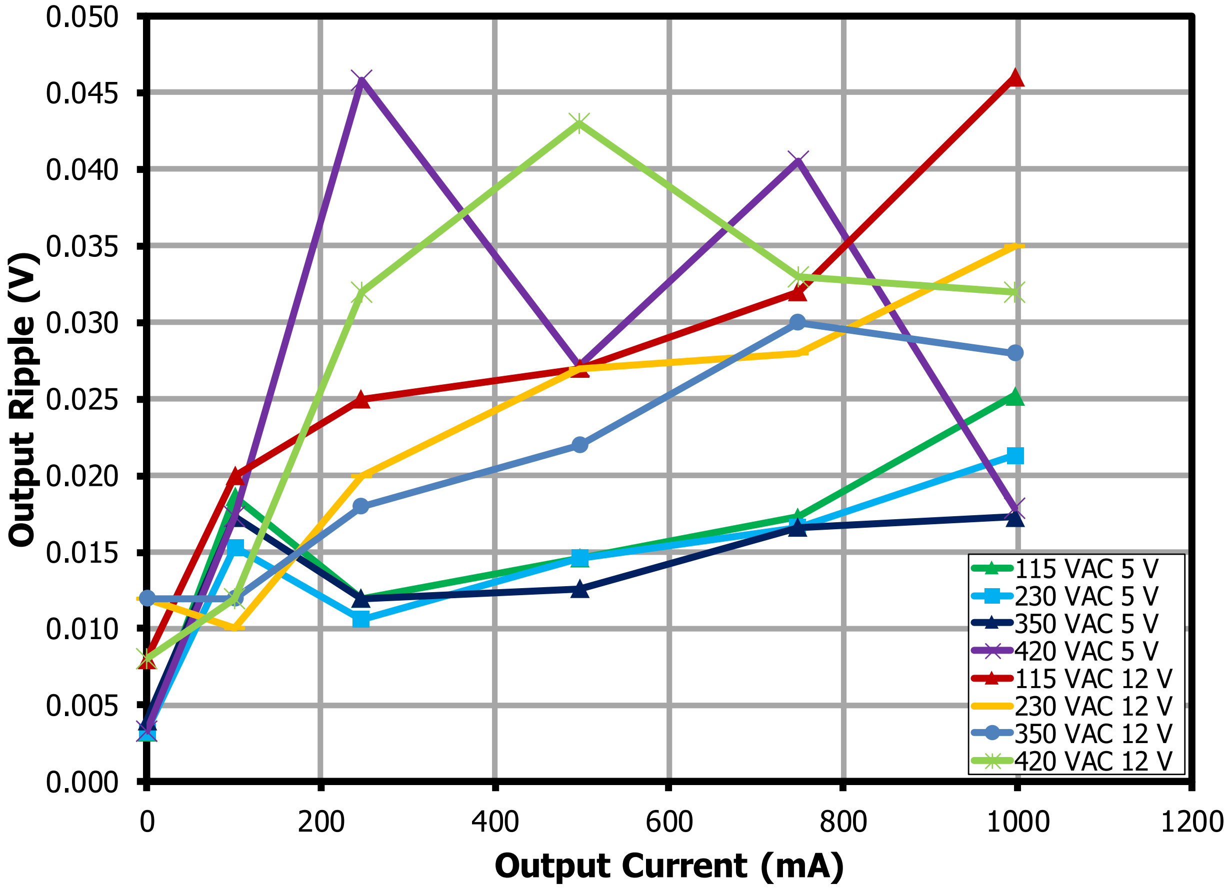


Figure 67 – Summary of Output Ripple vs. Load.

11.6 *Output Voltage Start-Up*

11.6.1 *100% Load*

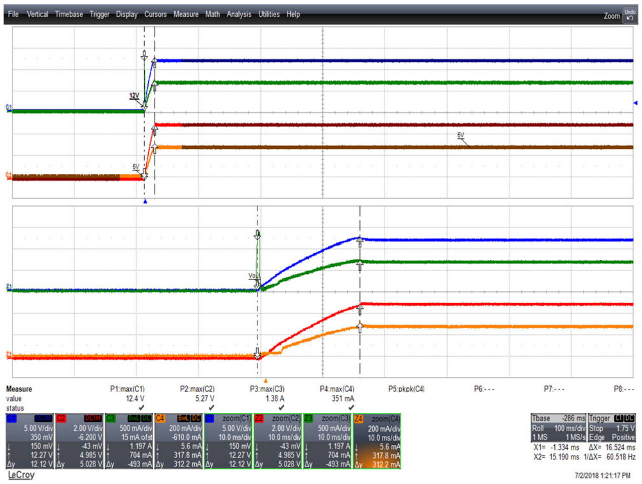


Figure 68 – 90 VAC, 60 Hz.
CH1: 12 V_{OUT}, 5 V / div., 100 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 100 ms / div.
CH3: 12 V I_{OUT}, 500 mA / div., 100 ms / div.
CH4: 5 V I_{OUT}, 200 mA / div., 100 ms / div.
Zoom: 10 ms / div.
12 V Tr = 16.5 ms.

Figure 69 – 265 VAC, 50 Hz.
CH1: 12 V_{OUT}, 5 V / div., 100 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 100 ms / div.
CH3: 12 V I_{OUT}, 500 mA / div., 100 ms / div.
CH4: 5 V I_{OUT}, 200 mA / div., 100 ms / div.
Zoom: 10 ms / div.
12 V Tr = 13 ms.

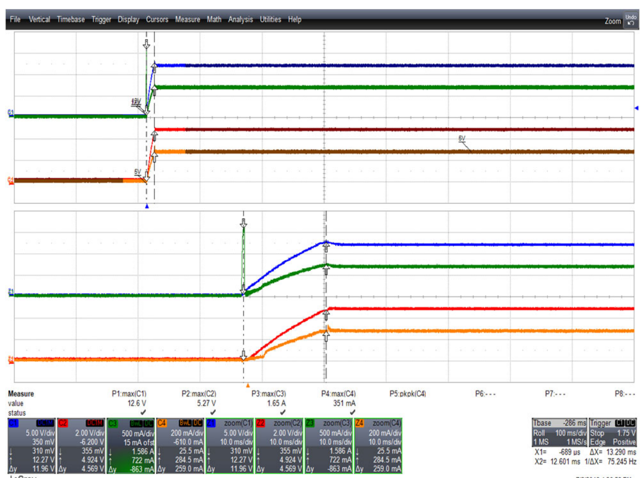


Figure 70 – 420 VAC, 50 Hz.
CH1: 12 V_{OUT}, 5 V / div., 100 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 100 ms / div.
CH3: 12 V I_{OUT}, 500 mA / div., 100 ms / div.
CH4: 5 V I_{OUT}, 200 mA / div., 100 ms / div.
Zoom: 10 ms / div.
12 V Tr = 13.3 ms.

11.6.2 *0% Load*

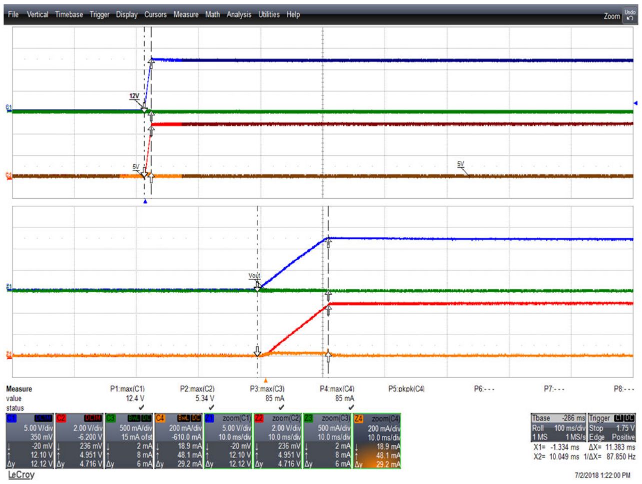


Figure 71 – 90 VAC, 60 Hz.
CH1: 12 V_{OUT}, 5 V / div., 100 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 100 ms / div.
CH3: 12 V I_{OUT}, 500 mA / div., 100 ms / div.
CH4: 5 V I_{OUT}, 200 mA / div., 100 ms / div.
Zoom: 10 ms / div.
12 V Tr = 11.4 ms.

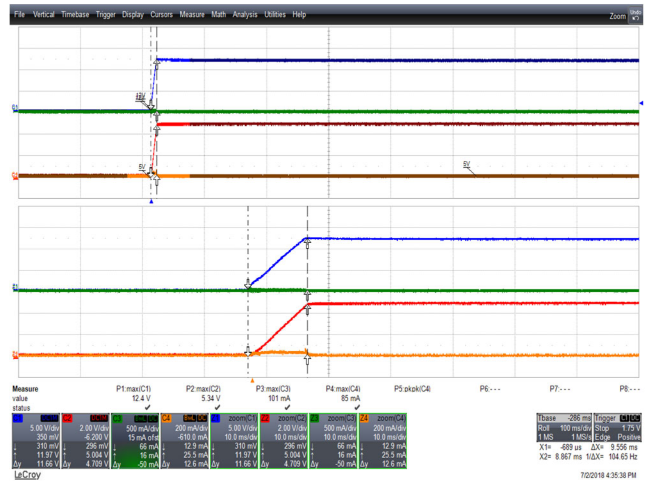


Figure 72 – 265 VAC, 50 Hz.
CH1: 12 V_{OUT}, 5 V / div., 100 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 100 ms / div.
CH3: 12 V I_{OUT}, 500 mA / div., 100 ms / div.
CH4: 5 V I_{OUT}, 200 mA / div., 100 ms / div.
Zoom: 10 ms / div.
12 V Tr = 9.6 ms.

Figure 73 – 420 VAC, 50 Hz.
CH1: 12 V_{OUT}, 5 V / div., 100 ms / div.
CH2: 5 V_{OUT}, 2 V / div., 100 ms / div.
CH3: 12 V I_{OUT}, 500 mA / div., 100 ms / div.
CH4: 5 V I_{OUT}, 200 mA / div., 100 ms / div.
Zoom: 10 ms / div.
12 V Tr = 9.3 ms.

11.7 *12 V Synchronous Rectifier MOSFET Waveforms*

11.7.1 *Start-up Operation*

11.7.1.1 100% Load (5 V / 0.3 A, 12 V / 0.7 A)

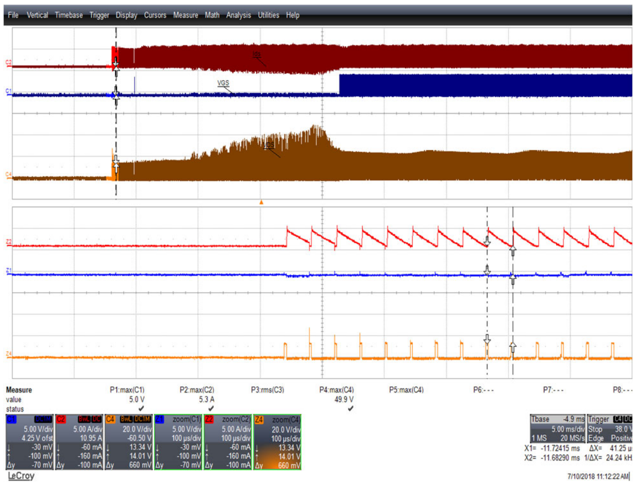


Figure 74 – 90 VAC, 60 Hz.
Ch1: SR V_{GS}, 5 V / div., 5 ms / div.
Ch2: SR I_{DS}, 5 A / div., 5 ms / div.
Ch4: SR V_{DS}, 20 V / div., 5 ms / div.
Zoom: 100 μs / div.
$SR_{VDS(MAX)}$: 49.9 V.
$SR_{IDS(MAX)}$: 5.3 A.

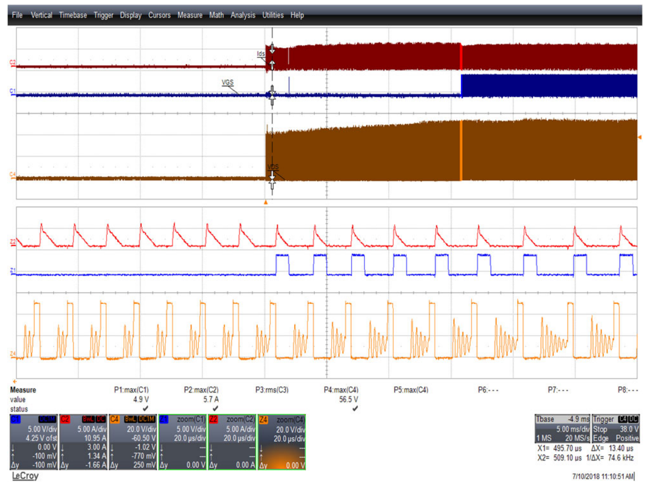


Figure 75 – 265 VAC, 50 Hz.
Ch1: SR V_{GS}, 5 V / div., 5 ms / div.
Ch2: SR I_{DS}, 5 A / div., 5 ms / div.
Ch4: SR V_{DS}, 20 V / div., 5 ms / div.
Zoom: 100 μs / div.
$SR_{VDS(MAX)}$: 56.5 V.
$SR_{IDS(MAX)}$: 5.7 A.

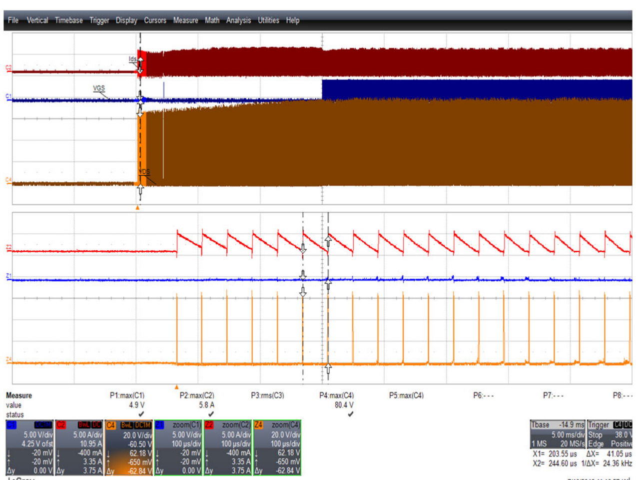


Figure 76 – 420 VAC, 50 Hz.
Ch1: SR V_{GS}, 5 V / div., 5 ms / div.
Ch2: SR I_{DS}, 5 A / div., 5 ms / div.
Ch4: SR V_{DS}, 20 V / div., 5 ms / div.
Zoom: 100 μs / div.
$SR_{VDS(MAX)}$: 80.4 V.
$SR_{IDS(MAX)}$: 5.8 A.

11.7.2 *Normal Operation*

11.7.2.1 100% LOAD (5 V / 0.3 A, 12 V / 0.7 A)

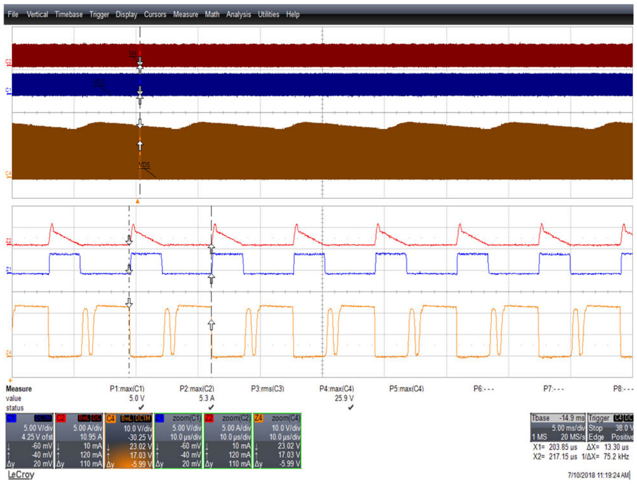


Figure 77 – 90 VAC, 60 Hz.
Ch1: SR V_{GS}, 5 V / div., 5 ms / div.
Ch2: SR I_{DS}, 5 A / div., 5 ms / div.
Ch4: SR V_{DS}, 20 V / div., 5 ms / div.
Zoom: 10 μs / div.
$SR_{VDS(MAX)}$: 25.9 V.
$SR_{IDS(MAX)}$: 5.3 A.

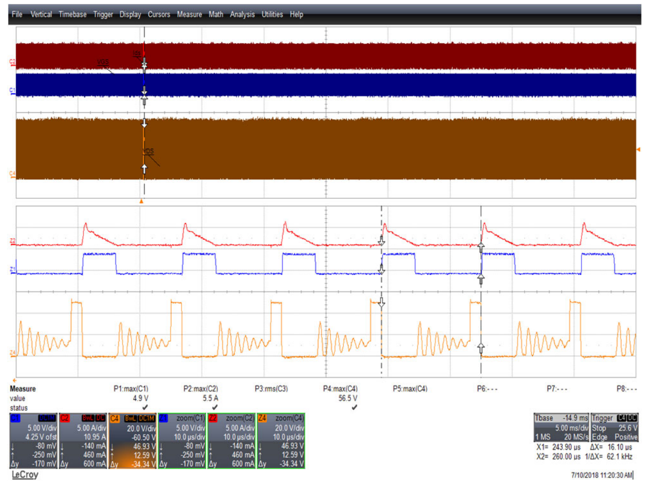


Figure 78 – 265 VAC, 50 Hz.
Ch1: SR V_{GS}, 5 V / div., 5 ms / div.
Ch2: SR I_{DS}, 5 A / div., 5 ms / div.
Ch4: SR V_{DS}, 20 V / div., 5 ms / div.
Zoom: 10 μs / div.
$SR_{VDS(MAX)}$: 56.5 V.
$SR_{IDS(MAX)}$: 5.5 A.

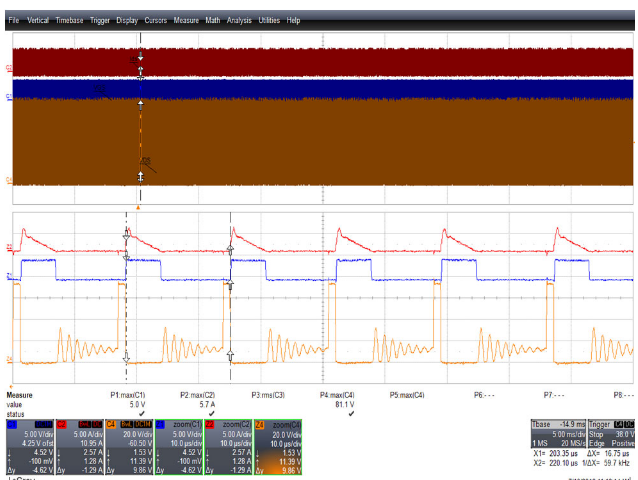


Figure 79 – 420 VAC, 50 Hz.
Ch1: SR V_{GS}, 5 V / div., 5 ms / div.
Ch2: SR I_{DS}, 5 A / div., 5 ms / div.
Ch4: SR V_{DS}, 20 V / div., 5 ms / div.
Zoom: 10 μs / div.
$SR_{VDS(MAX)}$: 81.1 V.
$SR_{IDS(MAX)}$: 5.7 A.

11.8 *5 V Synchronous Rectifier MOSFET Waveforms*

11.8.1 *Start-up Operation*

11.8.1.1 100% Load (5 V / 0.3 A, 12 V / 0.7 A)

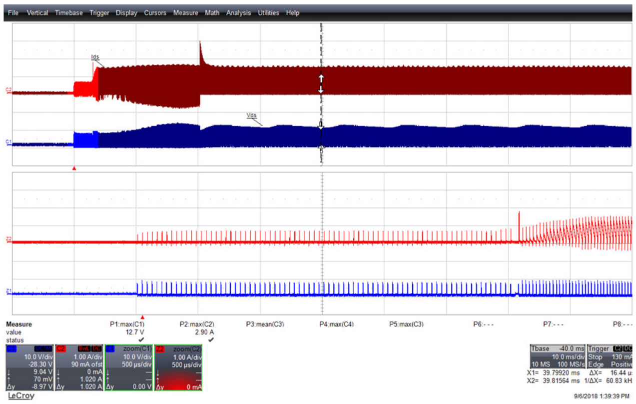


Figure 80 – 90 VAC, 60 Hz.
Ch1: SR V_{DS}, 10 V / div., 10 ms / div.
Ch2: SR I_{DS}, 1 A / div., 10 ms / div.
Zoom: 500 µs / div.
$SR_{VDS(MAX)}$: 12.7 V.
$SR_{IDS(MAX)}$: 2.9 A.

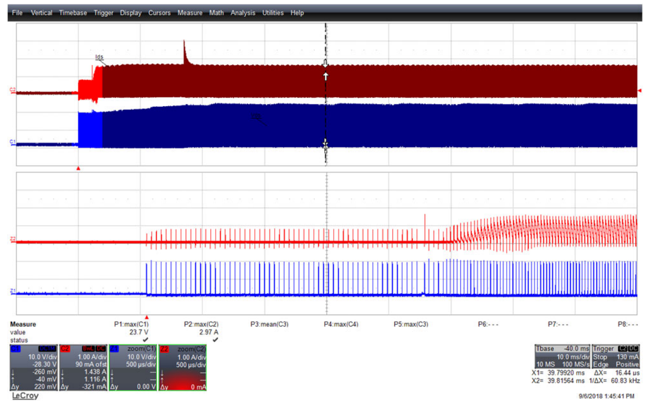


Figure 81 – 265 VAC, 50 Hz.
Ch1: SR V_{DS}, 10 V / div., 10 ms / div.
Ch2: SR I_{DS}, 1 A / div., 10 ms / div.
Zoom: 500 µs / div.
$SR_{VDS(MAX)}$: 23.7 V.
$SR_{IDS(MAX)}$: 3.0 A.

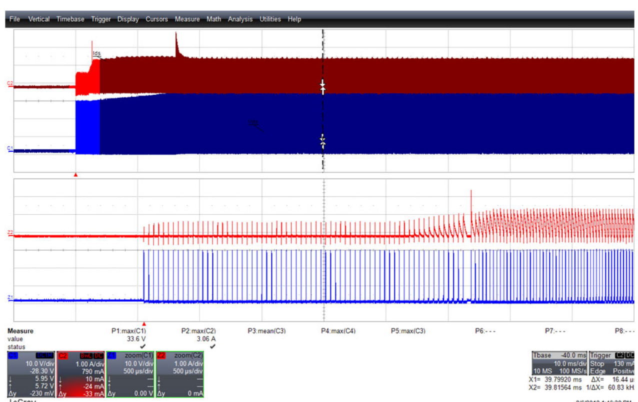


Figure 82 – 420 VAC, 50 Hz.
Ch1: SR V_{DS}, 10 V / div., 10 ms / div.
Ch2: SR I_{DS}, 1 A / div., 10 ms / div.
Zoom: 500 µs / div.
$SR_{VDS(MAX)}$: 33.6 V.
$SR_{IDS(MAX)}$: 3.1 A.

11.8.2 *Normal Operation*

11.8.2.1 100% Load (5 V / 0.3 A, 12 V / 0.7 A)

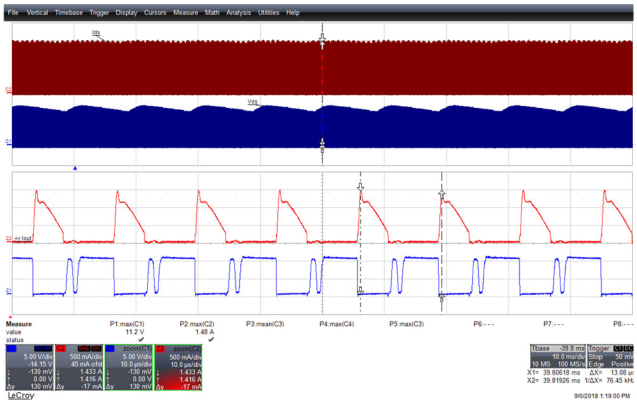


Figure 83 – 90 VAC, 60 Hz.
Ch1: SR V_{DS}, 5 V / div.,10 ms / div.
Ch2: SR I_{DS}, 0.5 A / div., 10 ms / div.
Zoom: 10 μs / div.
$SR_{VDS(MAX)}$: 11.2 V.
$SR_{IDS(MAX)}$: 1.5 A.

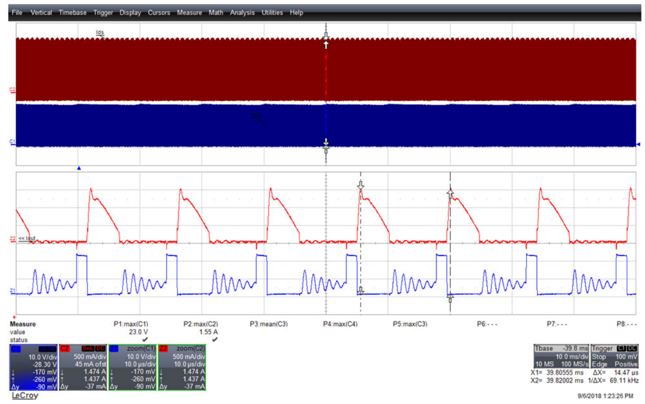


Figure 84 – 265 VAC, 50 Hz.
Ch1: SR V_{DS}, 10 V / div., 10 ms / div.
Ch2: SR I_{DS}, 0.5 A / div., 10 ms / div.
Zoom: 10 μs / div.
$SR_{VDS(MAX)}$: 23 V.
$SR_{IDS(MAX)}$: 1.6 A.

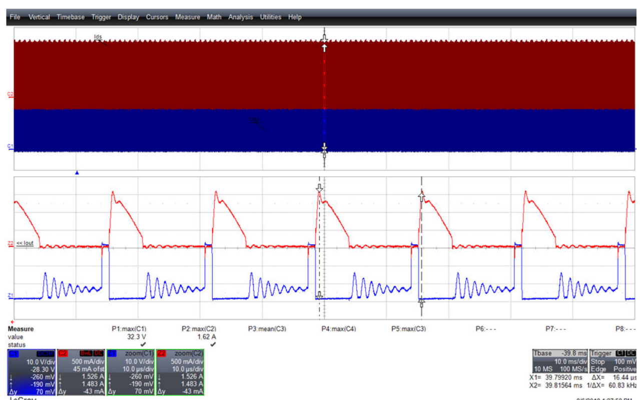


Figure 85 – 420 VAC, 50 Hz.
Ch1: SR V_{DS}, 10 V / div., 10 ms / div.
Ch2: SR I_{DS}, 0.5 A / div., 10 ms / div.
Zoom: 10 μs / div.
$SR_{VDS(MAX)}$: 32.3 V.
$SR_{IDS(MAX)}$: 1.6 A.

11.9 *Brown-In and Brown-Out*

11.9.1 *At 100%*

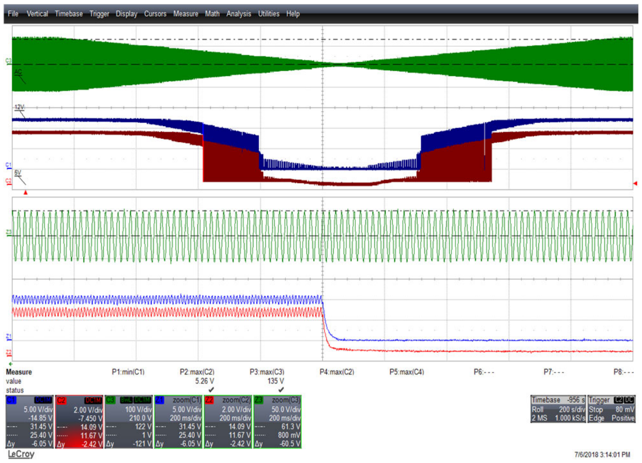


Figure 86 – 90 VAC, 60 Hz. Brown-Out.
Ch1: 12 V_{OUT}, 5 V / div., 200 s / div.
Ch2: 5 V_{OUT}, 2 V / div., 200 s / div.
Ch3: AC, 100 V / div., 200 s / div.
Zoom: 200 ms / div.
Brown-Out: 60.5 VAC.

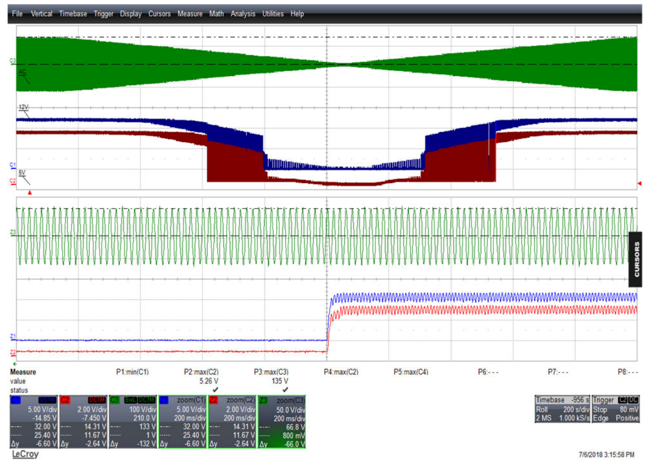


Figure 87 – 90 VAC, 60 Hz. Brown-In.
Ch1: 12 V_{OUT}, 5 V / div., 200 s / div.
Ch2: 5 V_{OUT}, 2 V / div., 200 s / div.
Ch3: VAC, 100 V / div., 200 s / div.
Zoom: 200 ms / div.
Brown-In: 66 VAC.

12 Output Short-Circuit

12.1 *5 V Output Shorted; 12 V @ 70 mA; 0 Ω Short*

Figure 88 – 90 VAC, 60 Hz.
Ch1: I_{DS}, 200 mA / div., 1 s / div.
Ch2: 12 V I_{OUT}, 1 A / div., 1 s / div.
Ch3: V_{DS}, 200 V / div., 1 s / div.
Ch4: 12 V_{OUT}, 5 V / div., 1 s / div.
Zoom: 20 ms / div.
Auto-restart ON Time: 45 ms.
Auto-restart OFF Time: 1.64 s.

Figure 89 – 265 VAC, 50 Hz.
Ch1: I_{DS}, 200 mA / div., 1 s / div.
Ch2: 12 V I_{OUT}, 1 A / div., 1 s / div.
Ch3: V_{DS}, 200 V / div., 1 s / div.
Ch4: 12 V_{OUT}, 5 V / div., 1 s / div.
Zoom: 20 ms / div.
Auto-restart ON Time: 45 ms.
Auto-restart OFF Time: 1.64 s.

Figure 90 – 420 VAC, 50 Hz.
Ch1: I_{DS}, 1 A /div., 1 s / div.
Ch2: 12 V I_{OUT}, 1 A / div., 1 s / div.
Ch3: V_{DS}, 200 V / div., 1 s / div.
Ch4: 12 V_{OUT}, 5 V / div., 1 s / div.
Zoom: 20 ms / div.
Auto-restart ON Time: 53 ms.
Auto-restart OFF Time: 1.64 s.

12.2 *12 V Output Shorted; 5 V @ 30 mA; 0 Ω Short*

Figure 91 – 90 VAC, 60 Hz.
Ch1: I_{DS}, 200 mA / div., 1 s / div.
Ch2: 12 V I_{OUT}, 1 A / div., 1 s / div.
Ch3: V_{DS}, 200 V / div., 1 s / div.
Ch4: 5 V_{OUT}, 5 V / div., 1 s / div.
Zoom: 20 ms / div.
Auto-restart ON Time: 45 ms.
Auto-restart OFF Time: 1.6 s.

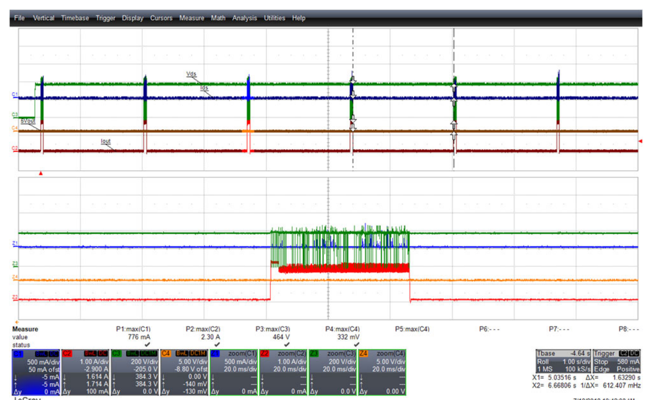


Figure 92 – 265 VAC, 50 Hz.
Ch1: I_{DS}, 500 mA / div., 1 s / div.
Ch2: 12 V I_{OUT}, 1 A / div., 1 s / div.
Ch3: V_{DS}, 200 V / div., 1 s / div.
Ch4: 5 V_{OUT}, 5 V / div., 1 s / div.
Zoom: 20 ms / div.
Auto-restart ON Time: 44 ms.
Auto-restart OFF Time: 1.63 s.

Figure 93 – 420 VAC, 50 Hz.
Ch1: I_{DS}, 500 mA / div., 1 s / div.
Ch2: 12 V I_{OUT}, 1 A / div., 1 s / div.
Ch3: V_{DS}, 200 V / div., 1 s / div.
Ch4: 5 V_{OUT}, 5 V / div., 1 s / div.
Zoom: 20 ms / div.
Auto-restart ON Time: 38 ms.
Auto-restart OFF Time: 4.5 s.

13 Output Overvoltage Protection

13.1 *Output Overvoltage Protection*

13.1.1 *At No-Load*

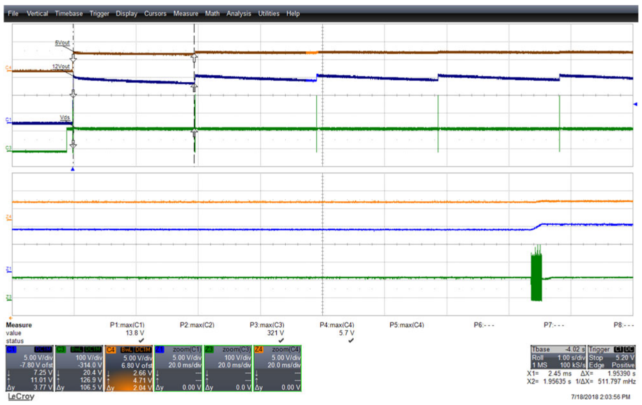


Figure 94 – 90 VAC, 60 Hz.
Ch1 12 V_{OUT}: 5 V / div., 1 s / div.
Ch3 V_{DS}: 100 V / div., 1 s / div.
Ch4 5 V_{OUT}: 5 V / div., 1 s / div.
Zoom: 20 ms / div.
12 V_{MAX}: 13.8 V.
5 V_{MAX}: 5.7 V.

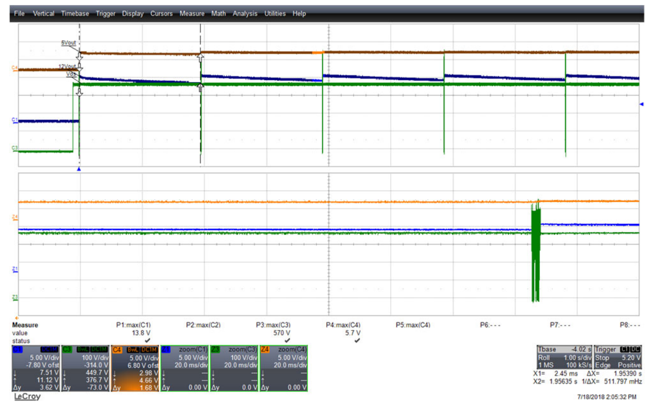


Figure 95 – 265 VAC, 50 Hz.
Ch1 12 V_{OUT}: 5 V / div., 1 s / div.
Ch3 V_{DS}: 100 V / div., 1 s / div.
Ch4 5 V_{OUT}: 5 V / div., 1 s / div.
Zoom: 20 ms / div.
12 V_{MAX}: 13.8 V.
5 V_{MAX}: 5.7 V.

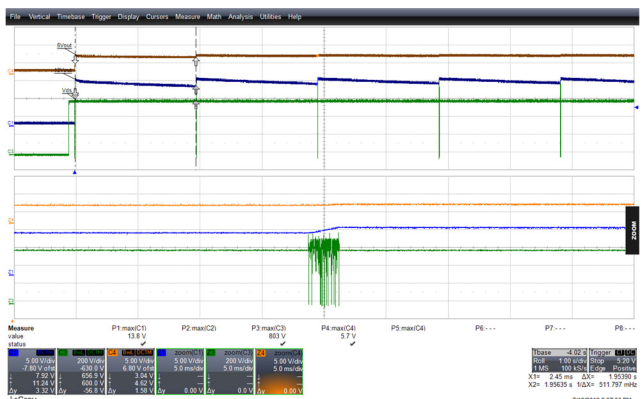


Figure 96 – 420 VAC, 50 Hz.
Ch1 12 V_{OUT}: 5 V / div., 1 s / div.
Ch3 V_{DS}: 100 V / div., 1 s / div.
Ch4 5 V_{OUT}: 5 V / div., 1 s / div.
Zoom: 5 ms / div.
12 V_{MAX}: 13.8 V.
5 V_{MAX}: 5.7 V.

13.2 *Line Overvoltage Protection*

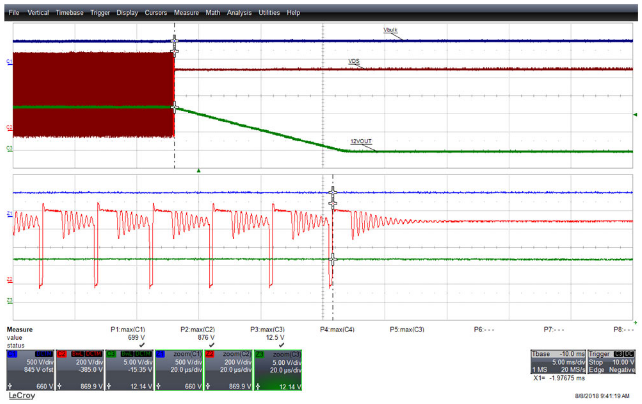


Figure 97 – 420 VAC, 50 Hz.
Ch1 V_{BULK}: 500 V / div., 5 ms / div.
Ch2 V_{DS}: 200 V / div., 5 ms / div.
Ch3 12 V_{OUT}: 5 V / div., 5 ms / div.
Zoom: 20 µs / div.
$V_{BULK(MAX)}$: 660 V.
$V_{DS(MAX)}$: 869.9 V.

14 Conductive EMI

14.1 *Neutral*

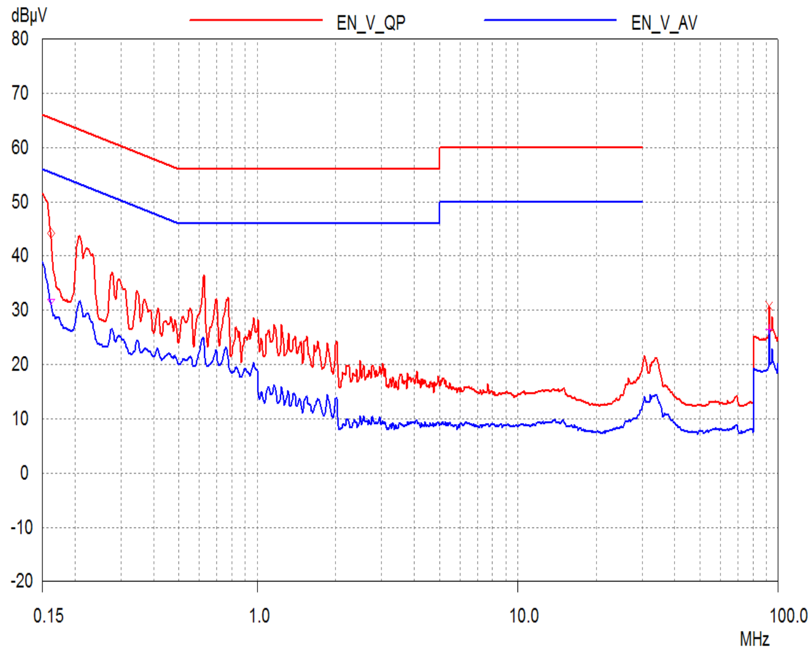


Figure 98 – Floating Ground EMI at 115 VAC, Neutral.

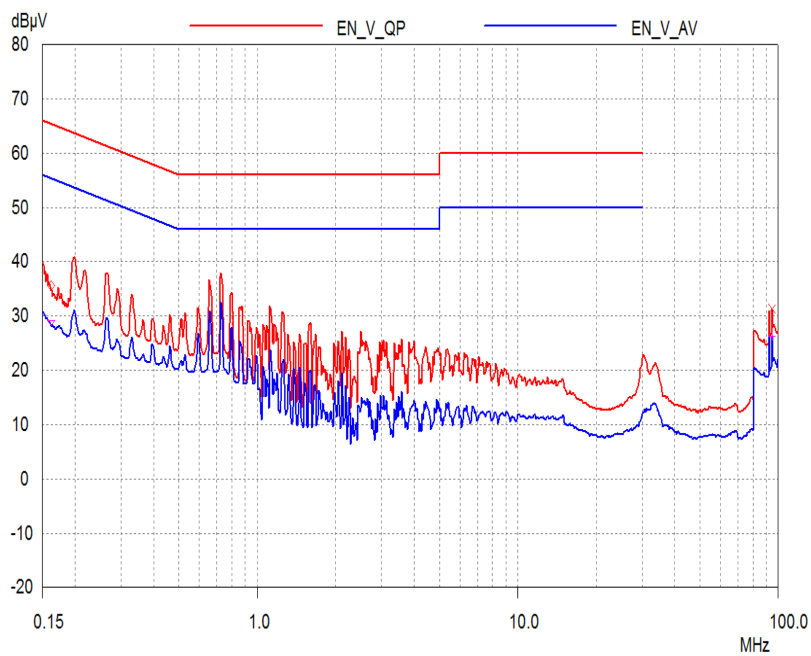


Figure 99 – Floating Ground EMI at 230 VAC, Neutral.

14.2 *Line*

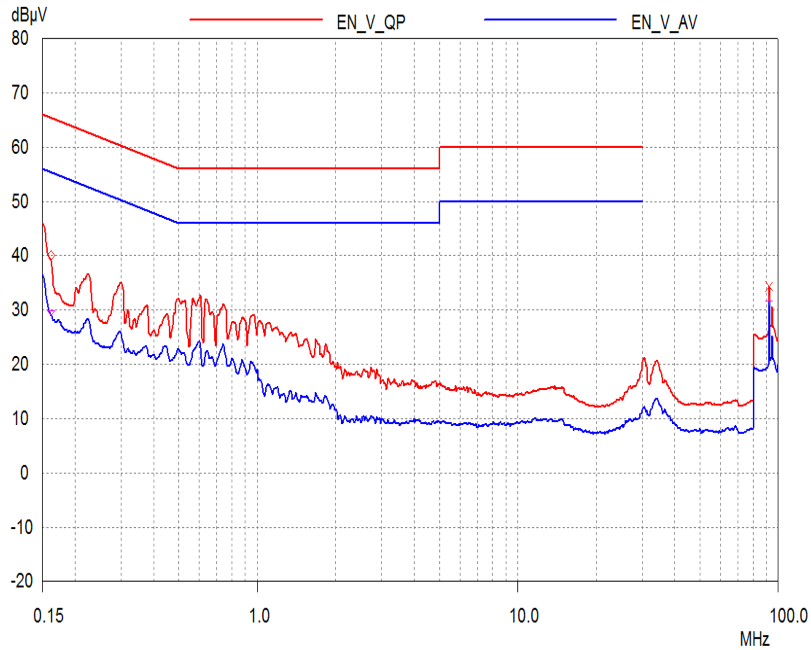


Figure 100 – Floating Ground EMI at 115 VAC, Line.

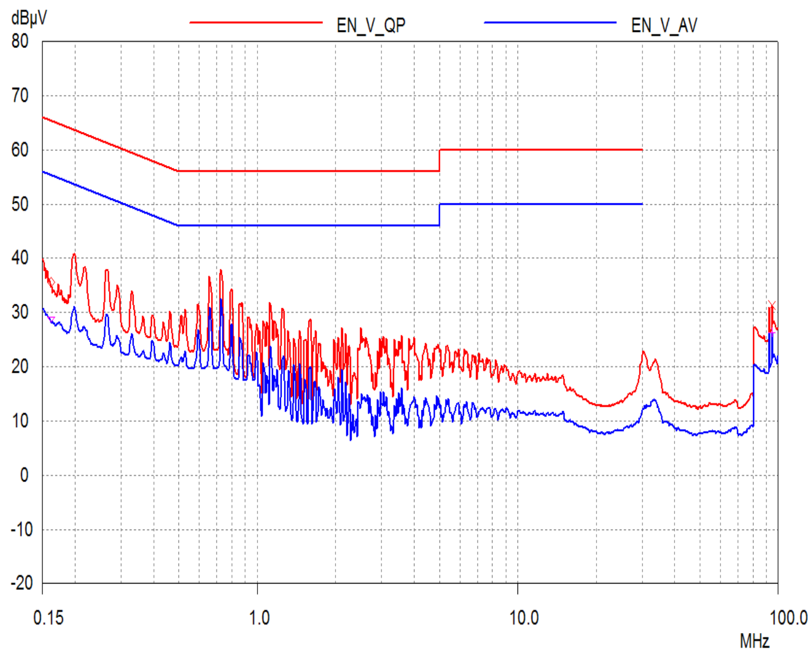


Figure 101 – Floating Ground EMI at 230 VAC, Line.

15 Line Surge

15.1 *Differential Surge Test Summary*

Surge Level (V)	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Remarks
D.M.		(2Ω source)		10 strikes each level
+2000	230	L to N	0	P1
+2000	230	L to N	90	P1
+2000	230	L to N	270	P1
-2000	230	L to N	0	P1
-2000	230	L to N	90	P1
-2000	230	L to N	270	P1

* P1:Pass

15.2 *Ring Wave Test Summary*

Surge Level (V) Comb. Wave	Input Voltage (VAC)	Injection Location	Injection Phase (°)	Test Result (Pass/AR/Fail)
C.M.		(12Ω source)		10 strikes each level
+3000	230	L, N to PE	0	P1
+3000	230	L, N to PE	90	P1
+3000	230	L, N to PE	270	P1
-3000	230	L, N to PE	0	P1
-3000	230	L, N to PE	90	P1
-3000	230	L, N to PE	270	P1
+4000	230	L, N to PE	0	P1
+4000	230	L, N to PE	90	P1
+4000	230	L, N to PE	270	P1
-4000	230	L, N to PE	0	P1
-4000	230	L, N to PE	90	P1
-4000	230	L, N to PE	270	P1
+5000	230	L, N to PE	0	P1
+5000	230	L, N to PE	90	P1
+5000	230	L, N to PE	270	P1
-5000	230	L, N to PE	0	P1
-5000	230	L, N to PE	90	P1
-5000	230	L, N to PE	270	P1
+6000	230	L, N to PE	0	P1
+6000	230	L, N to PE	90	P1
+6000	230	L, N to PE	270	P1
-6000	230	L, N to PE	0	P1
-6000	230	L, N to PE	90	P1
-6000	230	L, N to PE	270	P1

* P1:Pass

16 ESD

16.1 *Air Discharge*

Level (kV)	Positive Side (V+)	Negative Side (GND)
+8	0/10 AR	0/10 AR
-8	0/10 AR	0/10 AR
+10	0/10 AR	0/10 AR
-10	0/10 AR	0/10 AR
+12	0/10 AR	0/10 AR
-12	0/10 AR	0/10 AR
+14	0/10 AR	0/10 AR
-14	0/10 AR	0/10 AR
+16.5	0/10 AR	0/10 AR
-16.5	0/10 AR	0/10 AR

16.2 *Contact Discharge*

Level (kV)	Positive Side (V+)	Negative Side (GND)
+2	0/10 AR	0/10 AR
-2	0/10 AR	0/10 AR
4	0/10 AR	0/10 AR
-4	0/10 AR	0/10 AR
+6	0/10 AR	0/10 AR
-6	0/10 AR	0/10 AR
+8.8	0/10 AR	0/10 AR
-8.8	0/10 AR	0/10 AR

17 Revision History

Date	Author	Revision	Description & changes	Reviewed
28-Sep-18	DK	1.0	Initial Release	Apps & Mktg
21-Jul-22	KM	1.1	Added Transformer Supplier for T1	Apps & Mktg

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