



# UM90023

NEVB-NPS4053 load switch evaluation board

Rev. 1.0 — 7 August 2023

user manual

## Document information

Information	Content
Keywords	Load switch, evaluation board (EVB)
Abstract	The NEVB-NPS4053 evaluation board is a two-layer PCB containing the NPS4053 load switch device. The VIN and VOUT connections to the device and the PCB layout routing are capable of handling high continuous currents and provide a low-resistance pathway into and out of the device under test. Test point connections allow the EVB user to control the device with user-defined test conditions and make accurate RON measurements.

## 1. Introduction

The NEVB-NPS4053 is a dedicated PCB featuring the Nexperia load switch IC NPS4053, see [Fig. 1](#). The board is a 2-layer PCB with a substantial ground layer. The PCB layout routing is capable of handling high continuous currents and provide a low-resistance pathway into and out of the device under test. The test points are designed as separate voltage sensing connections on the PCB for accurate voltage and  $R_{ON}$  measurements where the test results are not influenced by voltage drops created by the load current. Solid input and output connections are provided with convenient test-point connection pins as well as robust solder pins. There are several connection terminals for GND and test points at the input and output of the load switch to allow a simple and very convenient connection of oscilloscope probes.

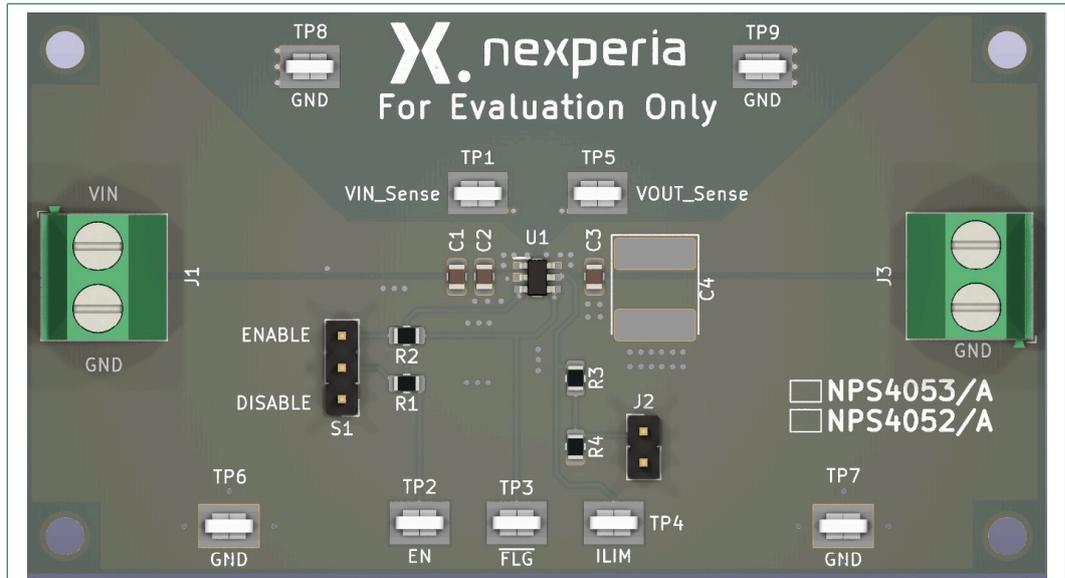


Fig. 1. NEVB-NPS4053; evaluation board for load switch IC NPS4053

### 1.1. Key Parameters

- EVB name = NEVB-NPS4053
- Device = NPS4053
- Input operating voltage range (VIN): 2.5 V to 5.5 V
- Rated currents of 2 A
- ON resistance ( $R_{ON}$ ): 55 m $\Omega$
- $\pm 6\%$  current accuracy at 1.2 A
- LIM pin protection: can be shorted to ground or be floating
- No body diode when disabled (no current path from OUT to IN)
- Active reverse input - output voltage protection
- Built in soft start
- UL 62368 Recognition
- 15 KV ESD protection per IEC 61000-4-2 (with external capacitance)

### 1.2. Features

- Input voltage can be supplied via the test points J1 (VIN), VIN can range from 2.5 V to 5.5 V.
- A test load can be connected to terminal J3 (VOUT).
- Alternatively, there are GND test points at TP6, TP7, TP8, and TP9.
- Decoupling capacitors are connected to VIN at the input of the EVB and close to the load switch IC. The same holds for the output.

- The enable pin (ON) has a smart pull-down resistor built in which disables the load switch if the enable pin is not terminated. For an activated load switch, the pull-down resistor is decoupled. This avoids current flowing through a pull-down that is not needed for the high state of the control input.
- VIN\_Sense (TP1) and VOUT\_Sense (TP5) are used when accurate measurements of the input or output are required. Make  $R_{ON}$  measurements using these Kelvin sense connections when measuring the voltage drop from VIN to VOUT.

## 2. Schematic

Fig. 2 shows the schematic diagram of the NEVB-NPS4053 evaluation board. The components, solder pins, connectors and test points described in the feature list above can be found here.

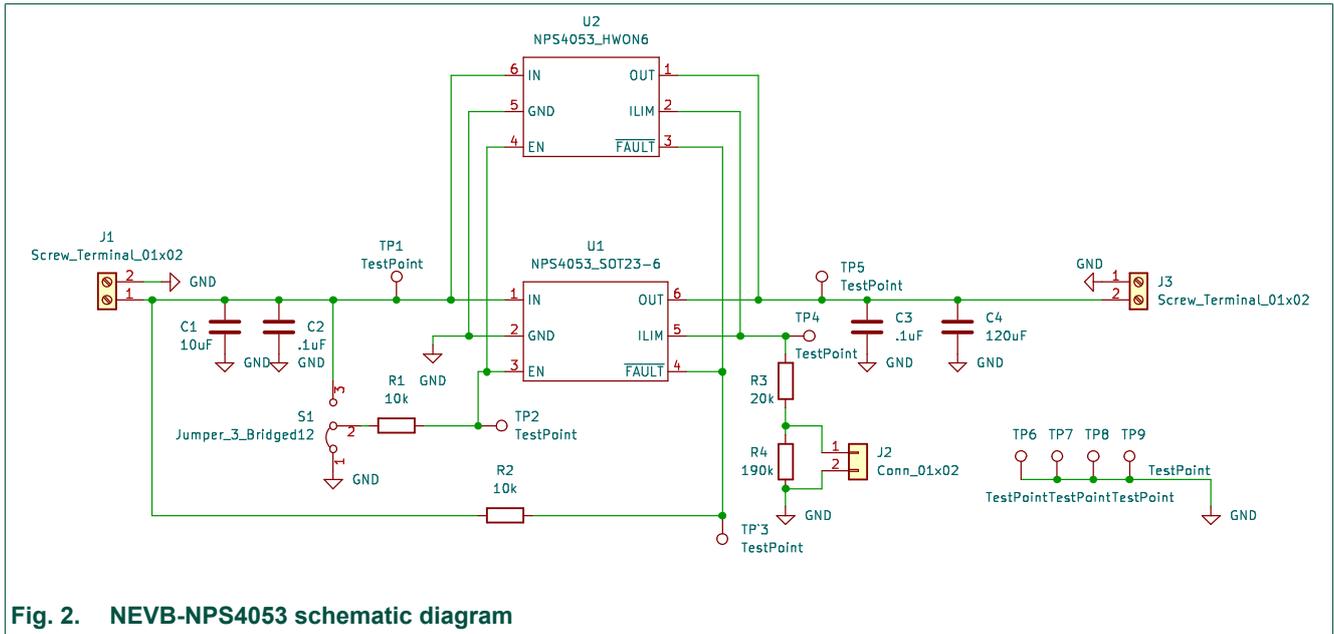
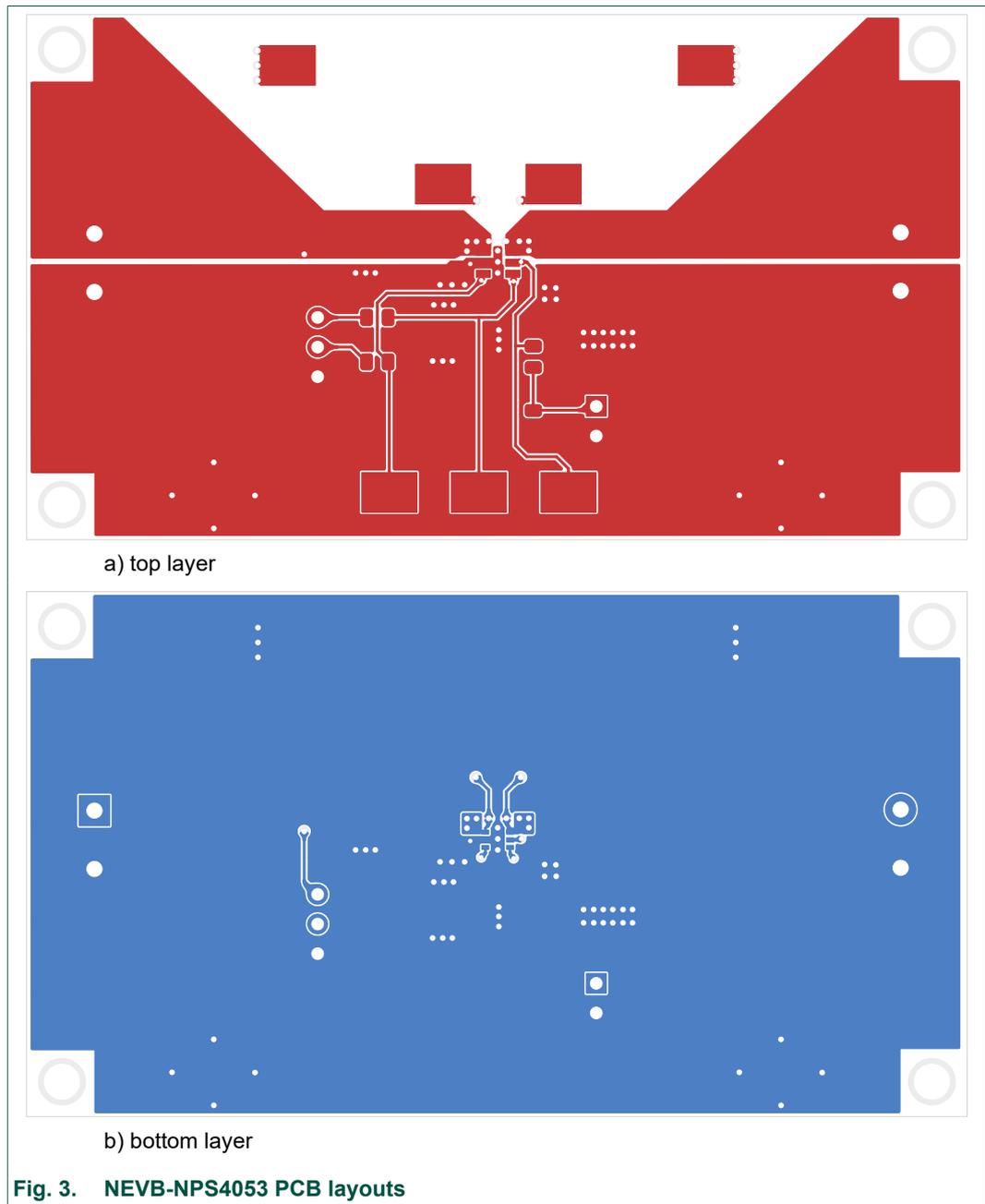


Fig. 2. NEVB-NPS4053 schematic diagram

### 3. PCB layout

Fig. 3 shows the PCB layout of the NEVB-NPS4053. The PCB has two layers, the top layer is shown in Fig. 3 a), the bottom layer is shown in Fig. 3 b).



## 4. Bill of Materials (BOM)

Table 1. NEVB-NPS4053 Bill of Materials

Component	Description	Designator	Quantity
PCB	Printed Circuit Board		1
CL21X106KOQNNNE	10 $\mu$ F +/-10% 16V X6S 2 0805	C1	1
LMK212SD104KG-T	0.1 $\mu$ F $\pm$ 10% 10 V Ceramic Capacitor 0805 (2012 Metric)	C2, C3	2
293D127X96R3D2TE3	120 $\mu$ F Molded Tantalum Capacitors 6.3 V 2917 (7343 Metric) 700 m $\Omega$	C4	1
1715022	TERM BLK 2POS SIDE ENTRY 5 mm PCB	J1, J3,	2
5-146278-2	CONN HEADER VERT 2POS 2.54 mm	J2	1
RNCS0805BKE10K0	RES 10 K $\Omega$ 1% 1/8W 0805	R1, R2	2
ERA-6AEB203V	RES 20 K $\Omega$ 0.1% 1/8W 0805	R3	1
RC0805FR-07191KL	RES 191 K $\Omega$ 1% 1/8W 0805	R4	1
5-146278-3	CONN HEADER VERT 3POS 2.54 mm	S1	1
5019	PC TEST POINT MINIATURE	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9	9
NPS40XX	NPS4053 TSOP6 package [1]	U1	DNP
NPS40XX	NPS4053 WSON6 package [1]	U2	1

[1] The NEVB-NPS4053 can accommodate the WSON6 or the TSOP-6 package. The WSON6 package is located on the back of the EVB and the TSOP-6 package is located on the front.

## 5. Set up and operation

The NEVB-NPS4053 board is quite easy to set up and operate. This chapter gives some instructions for proper use.

### 5.1. Input supply

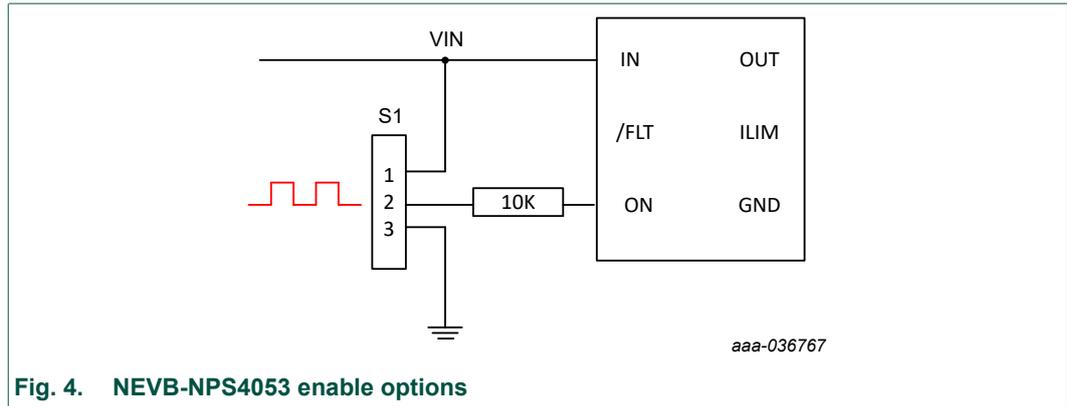
The input voltage source VIN is connected to the points J1(IN), VIN. This is where the positive lead is connected. The points J1(GND), J3 (GND), TP6, TP7, TP8, TP9. are the ground connections. For experiments with higher current, the cables from the power supply to the EVB should be adequate regarding resistance in order to avoid higher voltage losses from the power supply to the load switch board.

### 5.2. Load switch output

Loads at the output can be connected via the test points labeled OUT. The direct ground connections are appropriately labeled across the EVM

### 5.3. Enable control

Connector S1 connects the enable input EN of the load switch IC to either VIN or GND, hence turning the load switch IC on or off. External control signals can be applied via S1 pin 2 from an external function generator for example see [Fig. 4](#). The limits from the data sheet must be obeyed for the voltage applied at the enable pin. Furthermore, make sure S1 pin 2 isn't jumpered to Pins 1 or 3.



### 5.4. Voltage sense test points

The NEVB-NPS4053 includes Kelvin sense test points for VIN and VOUT, these are labeled VIN\_Sense and VOUT\_Sense. These test pins allow for precise measurement of the input and output voltages present at the package pins of the load switch IC. At these test points there is no influence from voltage drop due to the impedance of the PCB traces.  $R_{ON}$  can be evaluated with exact results at these test points as:

$$R_{ON} = \frac{(VIN\_Sense - VOUT\_Sense)}{I_{OUT}} \quad (1)$$

### 5.5. Start-up operation

To start operating the NEVB-NPS4053, connect a power supply with 2.5 V to 5.5 V to VIN. The load switch needs to be enabled by applying a jumper to S1 pins 3 and 2 or applying a high-level input signal to the enable pin as described in [Section 5.3](#). With a load connected to the VOUT terminals, a maximum continuous output current of 2 A can be supported by the NPS4053.

## 6. Test configurations

### 6.1. Measurement set-up for on-resistance

The NEVB-NPS4053 supports accurate measurement of the load switch IC on-resistance. Using a voltmeter, DC power supply, and a load connected at the output, on-resistance measurements of the IC can be made. A typical load current for this measurement is around 200 mA.

[Fig. 5](#) shows connections for a voltmeter, input voltage source and load.

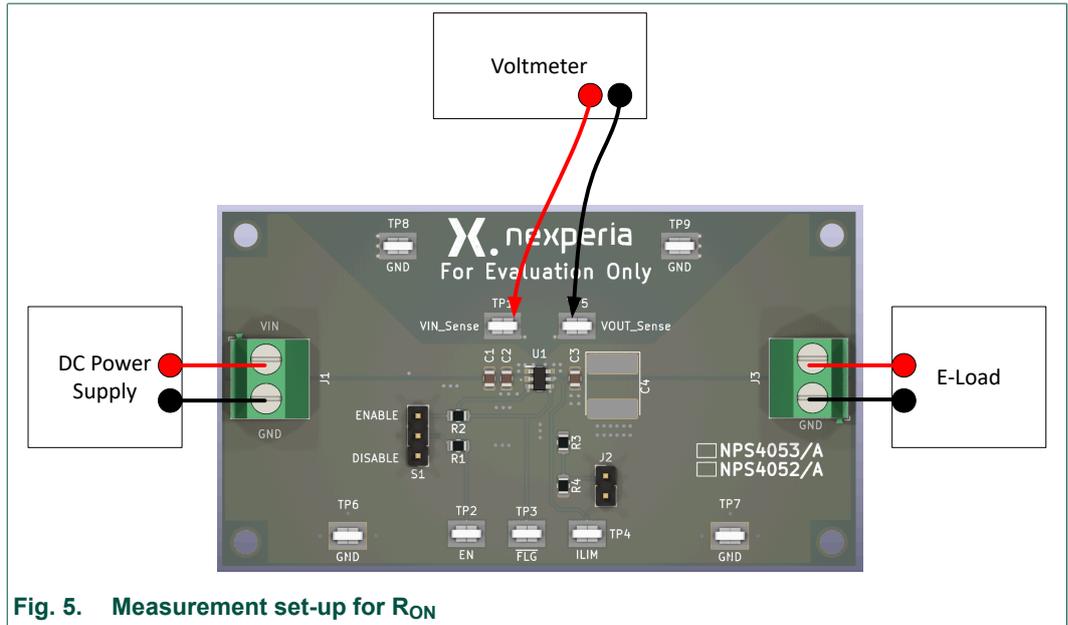


Fig. 5. Measurement set-up for  $R_{ON}$

### 6.2. Dynamic parameter testing

Dynamic parameters like the smooth turn-on of the NPS4053 can be measured at VOUT\_Sense using an oscilloscope. At S1 pin 2 the enable signal can be accessed and used as trigger signal.

Fig. 6 shows the oscilloscope connection points for measurement of VIN and VOUT with triggering from the enable input. With the same set-up the fall time of VOUT can be measured.

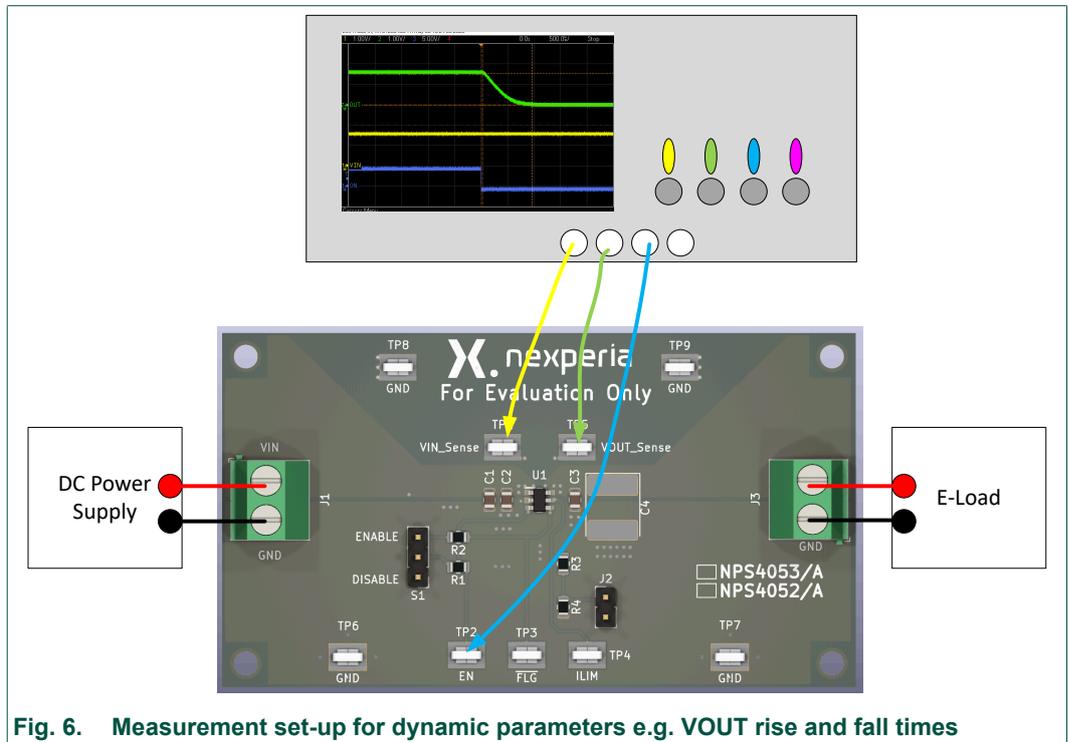


Fig. 6. Measurement set-up for dynamic parameters e.g. VOUT rise and fall times

## 7. Revision history

Table 2. Revision history

Revision number	Date	Description
1.0	2023-08-07	Initial version.

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**List of Tables**

Table 1. NEVB-NPS4053 Bill of Materials..... 5  
Table 2. Revision history.....8

## List of Figures

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Fig. 1. NEVB-NPS4053; evaluation board for load switch IC NPS4053.....	2
Fig. 2. NEVB-NPS4053 schematic diagram.....	3
Fig. 3. NEVB-NPS4053 PCB layouts.....	4
Fig. 4. NEVB-NPS4053 enable options.....	6
Fig. 5. Measurement set-up for RON.....	7
Fig. 6. Measurement set-up for dynamic parameters e.g. VOUT rise and fall times.....	7

## Contents

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<b>1. Introduction</b> .....	<b>2</b>
1.1. Key Parameters.....	2
1.2. Features.....	2
<b>2. Schematic</b> .....	<b>3</b>
<b>3. PCB layout</b> .....	<b>4</b>
<b>4. Bill of Materials (BOM)</b> .....	<b>5</b>
<b>5. Set up and operation</b> .....	<b>5</b>
5.1. Input supply.....	5
5.2. Load switch output.....	5
5.3. Enable control.....	5
5.4. Voltage sense test points.....	6
5.5. Start-up operation.....	6
<b>6. Test configurations</b> .....	<b>6</b>
6.1. Measurement set-up for on-resistance.....	6
6.2. Dynamic parameter testing.....	7
<b>7. Revision history</b> .....	<b>8</b>
<b>8. Legal information</b> .....	<b>9</b>

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