Using NCP51561 to Efficiently Drive SiC MOSFETs

AND90063/D

This application note provides guidance on how to design the power supply topology of NCP51561 isolated gate driver when using Silicon Carbide (SiC) MOSFETs.

As new power transistors, such as SiC MOSFETs, are being increasingly used in power electronics systems, it has become necessary to use special drivers. Isolated gate drivers are designed for the highest switching speeds and system size constrains required by technologies such as SiC (Silicon carbide) and GaN (Gallium nitride), by providing reliable control over IGBT and MOSFET. Many designers in the power electronic industry are already expert users of MOSFET, and IGBT in power converter designs. However, 1200 V and 1700 V SiC MOSFETs have becomes a real alternative to using IGBTs in power applications.

This application note focuses on optimization the design of gate driving voltage for speed to minimize switching losses and to get the full benefit of the devices.

There are many similarities between SiC MOSFETs and Si MOSFETs. However, some of the challenges faced by the designers of SiC MOSFETs is the control of the gate threshold voltage. SiC MOSFETs show more dependence upon gate voltage at the recommended gate drive voltage than silicon devices. SiC MOSFETs require a higher positive gate drive voltage (+20 V) and, depending on the application, a negative OFF gate voltage in the −2 V to −6 V range because it exhibits lower Vgs threshold that could lead to unwanted Turn−ON of the SiC MOSFET. For more details, you can refer to document in note [1].

The following is a short summary of the minimum gate driving requirements:

- Similarly to traditional Si MOSFET drivers, deliver high peak currents at turn−on and turn−off to quickly charge/discharge the C_{GS} and C_{GD} capacitances.
- SiC MOSFETs have a lower $R_{DS(on)}$ than Si MOSFETs. They are normally driven at a higher gate voltage, typically −5 V to 20 V, to enhance $R_{DS(on)}$ and switching speed. In order to achieve the lowest $R_{DS(on)}$ and the fastest turn−off speed and to provide dV/dt immunity, the SiC MOSFET gate driver should provide 20 V to 22 V and about −5 V respectively during the ON and OFF state of SiC MOSFETs.
- The body diode of a SiC MOSFET has a high voltage drop (about 4 V), but a low minority carrier lifetime. They have a significantly faster recovery and a lower recovery charge than that of Si MOSFETs.
- The output switching current (dI/dt) is significantly higher with SiC MOSFETs than with Si MOSFETs. This affects DC bus ringing, EMI, and output stage losses.
- Mitigate the negative feedback effect of the source inductance by using a low inductance package – also consider co−packaging later.

For more details, you can refer to document in note [2].

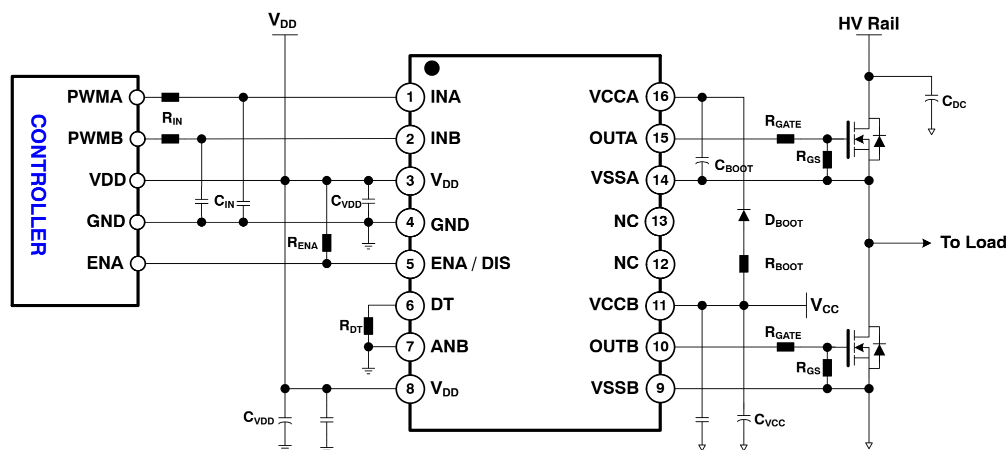


Figure 1. Typical Application Circuit of the NCP51561

APPLICATINS INFORMATION

The NCP51561 are isolated dual−channel gate drivers with 4−A/8−A source and sink peak current respectively. It implements reinforced isolation and can withstand 8 kV Peak and 5.7 kV_{RMS} isolation voltage and >150 V/ns common mode transient immunity (CMTI).

Considering of the Gate Voltage for SiC MOSFET

The design of a SiC MOSFET gate driver is much like the design of a standard IGBT or silicon MOSFET driver.

SiC IGBTs gate voltage is typically driven from −8 V in the OFF state to +15 V in the ON state. For SiC MOSFETs, the voltage varies slightly to +18 V or +20 V in the ON state and –5 V in the OFF state. It is highly recommended to use a negative bias gate drive with SiC MOSFETs in switching applications because there could be ringing in the gate−source drive voltage of the power transistor during high di/dt and dv/dt switching cause of parasitic inductances are introduced by non−ideal PCB layout.

Driving the SiC MOSFET more aggressively at +20 V minimizes switching losses and improves the surge current rating for the SiC device, but it puts a greater voltage stress on the gate, which can affect the long−term reliability of the device. With slower devices, such as silicon MOSFETs and IGBTs, a negative bias gate drive is commonly used in power applications. There are two reasons for this:

- *Gate Drive Impedance* −The gate driver's function is to turn the MOSFET ON and OFF (usually quickly) in order to reduce losses. To avoid cross conduction losses due to the Miller effect or due to slow switching with some loads, it is important for the driver to assert the off state with a lower impedance than the on−state drive on the opposing transistor. The negative gate drive margin plays an important part in reducing these losses
- *Source Inductance* − This is the inductance shared by the gate driver current loop and the output current loop. The negative gate drive voltage margin combined with the source lead inductance have a direct effect on the switching speed of the output under load. This is due to the source degeneration effect of the source inductance (the source lead inductance couples the output switching current back to the gate drive, slowing the gate drive)

The power supply of gate drive should be rated for at least 50 V/ns or above for the higher speed of SiC MOSFETs application. Most are not.

Gate Driver Specification for SiC MOSFET

The following is a short list of the minimum gate driving requirements: Compensating for the low gain while achieving efficient. High−speed switching imposes the following critical requirements for a SiC gate drive circuit:

- dv/dt transient immunity: At least ±50 V/ns across the entire temperature range SiC MOSFETs are tailored to switch fast and operate at high frequencies, hence the intrinsic device dv/dt is higher than that observed on silicon IGBTs
- A SiC MOSFET specifies an asymmetrical max/min V_{GS} near the range of +25 V/±10 V. The gate drive circuit must be capable of providing nearly the full range of 35 V, V_{GS} swing to take full advantage of the SiC MOSFET performance benefits. Given that the gate charge required to switch the device is low, the higher voltage swing doesn't affect the required gate drive power.
  Most SiC MOSFETs will perform best when driven between −5 V > V_{GS} > 20 V. To cover the widest range of available SiC MOSFETs, the gate drive circuit should be able to withstand VDD = 25 V and VEE = −10 V
- V_{GS} must have fast rise and fall edges, on the order of a few ns
- Must be able to source high peak gate current on the order of several amps, across the entire Miller plateau region
- Sink current capability is driven by the need to provide a very low impedance hold−down or “clamp” as the V_{GS} falls below the Miller plateau. The sink current rating should exceed what would be required by merely having to discharge the input capacitance of a SiC MOSFET
- Must have VDD under−voltage lockout (UVLO) level that is matched to the requirement that V_{GS} > ~16 V before switching begins
- Low parasitic inductance for high−speed switching
- Small driver package able to be located as close as possible to the SiC MOSFET

Considering of Application Circuits with Output Stage Negative Bias for SiC MOSFET

SiC MOSFET unique operating characteristics need to be carefully considered to fully benefits from SiC characteristics. The gate driver needs to be capable of providing +20 V and −2 V to −5 V negative bias with minimum output impedance and high current capability.

When parasitic inductances are introduced by non−ideal PCB layout and long package leads (e.g. TO−220 and TO−247 type packages), there could be ringing in the gate−source drive voltage of the power transistor during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, there is the risk of unintended turn−on and even shoot−through. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. Negative voltage can improve the noise tolerance of SiC MOSFET to suppress turning it unintentionally. The negative gate−source voltage makes the capacitance of Cgd becoming lower, which can reduce the ringing voltage. Below are a few examples of implementing negative gate drive bias.

The first example with negative bias with two isolated−bias power supplies as shown in Figure 2. Power supply VHx determines the positive drive output voltage and VLx determines the negative turn−off voltage for each channels. This solution requires more power supplies than the conventional bootstrapped power supply example; however, it provides more flexibility when setting the positive, VHx, and negative, VLx, rail voltages.

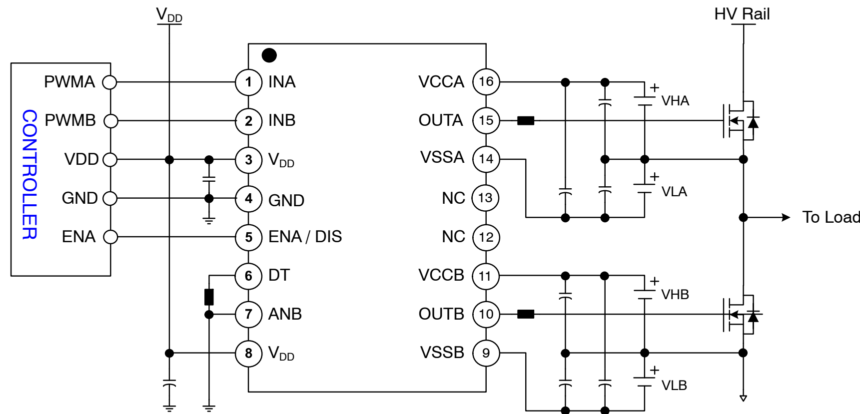


Figure 2. Negative Bias with Two Isolated−Bias Power Supplies

Figure 3 shows another example with negative bias turn−off on the gate driver using a Zener diode on an isolated power supply. The negative bias set by the voltage of Zener diode. For example, if the isolated power supply, VHx for each channels, the turn−off voltage will be –5.1 V and turn−on voltage will be 20 V – 5.1 V ≈ 15 V. Moreover, this configuration could easily be changed negative bias by a using different Zener diode with the same 20 V isolated power supply.

This configuration needs two isolated power supplies for a half−bridge configuration, but this scheme is very simple.

However, it has the disadvantage of having a steady state power consumption from R_{Zx}. Therefore, one should be careful in selecting the R_{Zx} values. It is recommended that R_{Zx} allow the minimal current flow to stabilize the Zener clamping voltage (e.g. I_Z : 5 mA ~ 10 mA).

Typical recommended values are in the few kohm range (e.g. 1 kΩ ~ 2 kΩ) of SiC MOSFETs application.

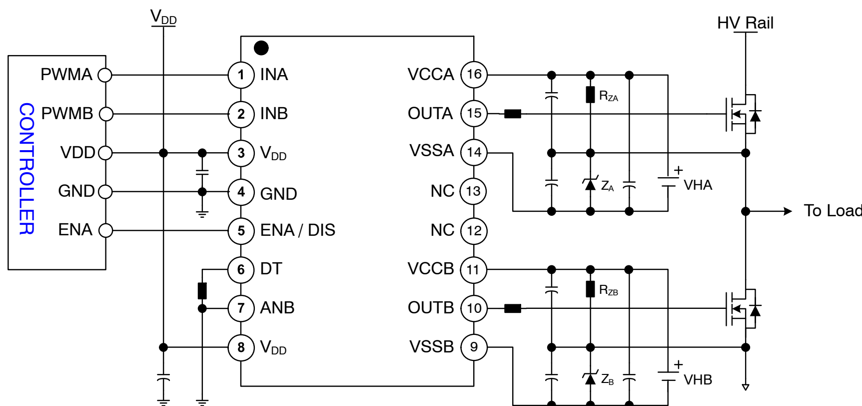
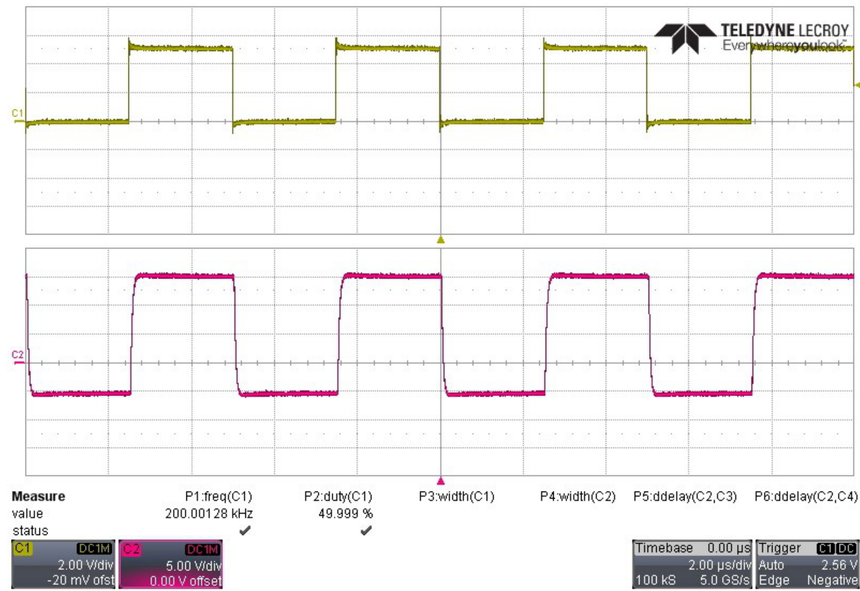


Figure 3. Negative Bias with Zener Diode on Single Isolated−Bias Power Supply

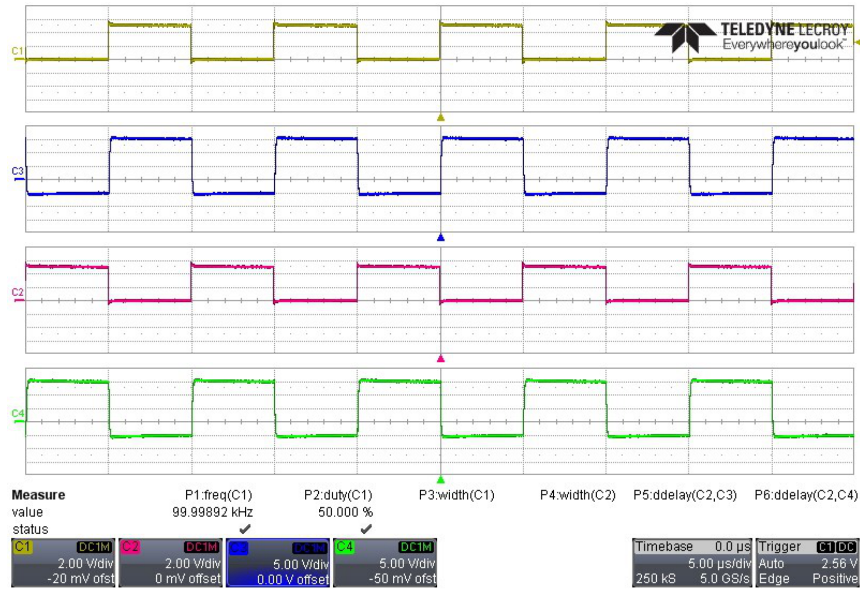
Test Results

SiC MOSFET unique operating characteristics need to be carefully considered to fully benefits from SiC characteristics. The gate driver needs to be capable of providing +20 V and −2 V to −5 V negative bias with minimum output impedance and high current capability.



CH1: INPUT [2 V/div], and CH2: OUTPUT [5 V/div]

Figure 4. Experimental Waveforms of Negative Bias with Zener Diode on Single Isolated Power Supply



CH1: INA [2 V/div], CH2: INB [2 V/div], CH3: OUTA [5 V/div], and CH4: OUTB [5 V/div]

Figure 5. Experimental Waveforms of Negative Bias with Zener Diode on Single Isolated Power Supply

Reference

[1] Micro Semiconductor Application note, “Design Recommendations for SiC MOSFETs”

[2] **onsemi** TND6237/D, “SiC MOSFETs: Gate Drive Optimization” https://www.onsemi.com/pub/Collateral/TND6237−D.PDF

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