1   About this document

This Product brief is intended to provide overview/summary information for the purpose of evaluating a product for design suitability. It is intended for quick reference only and should not be relied upon to contain detailed and full information.

Some of the content in this product brief is extracted from the product's full data sheet. In case of any inconsistency or conflict, the full data sheet shall prevail.

For detailed and full information, see the relevant FS26 full data sheet, available via the NXP Secure Files content interface.

2   General description

Devices in the FS26 automotive safety System Basis Chip (SBC) family are designed to support entry and mid-range safety microcontrollers, like those in the S32K3 series. FS26 devices have multiple power supplies and the flexibility to work with other microcontrollers targeting automotive electrification. Possible FS26 applications include power train, chassis, safety and low-end gateway technology.

This family of devices consist of several versions that are pin to pin and software compatible. These versions support a wide range of applications with Automotive Safety Integrity Levels (ASIL) B or D, offering choices in number of output rails, output voltage settings, operating frequencies, power up sequencing, and integrated system level features.

The FS26 features multiple switch mode regulators and low dropout (LDO) voltage regulators to supply the microcontroller, sensors, peripheral ICs and communication interfaces. It offers a high precision reference voltage supply for the system, and for two independent tracking regulators. The FS26 also offers various functionality for system control and diagnostics, including an analog multiplexer, General Purpose Input/Outputs (GPIOs), and selectable wakeup events from I/O, long duration timer or Serial-Peripheral Interface (SPI) communication.

The FS26 is developed in compliance with the ISO26262 standard, and includes enhanced safety features with multiple fail-safe outputs. It uses the latest on-demand latent fault monitoring, and can be part of a safety-oriented system partitioning scheme covering both ASIL B and ASIL D safety integrity levels.
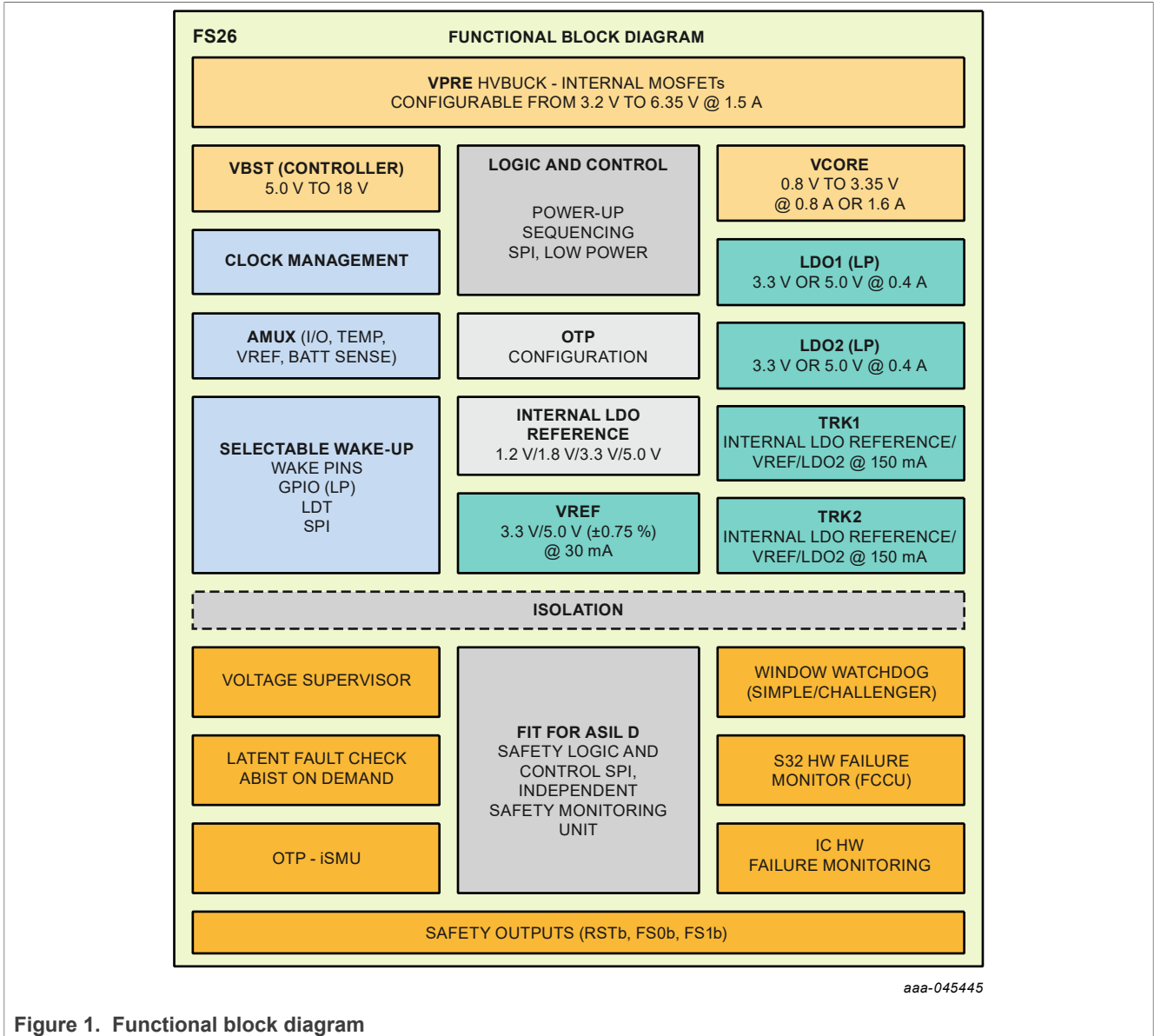
PB_FS26

Product brief

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Rev. 2 — 1 June 2022

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2 / 30

FS26	FUNCTIONAL BLOCK DIAGRAM

VPRE HVBUCK - INTERNAL MOSFETs
CONFIGURABLE FROM 3.2 V TO 6.35 V @ 1.5 A

VBST (CONTROLLER)
5.0 V TO 18 V

LOGIC AND CONTROL
POWER-UP SEQUENCING
SPI, LOW POWER

VCORE
0.8 V TO 3.35 V
@ 0.8 A OR 1.6 A

CLOCK MANAGEMENT

LDO1 (LP)
3.3 V OR 5.0 V @ 0.4 A

AMUX (I/O, TEMP, VREF, BATT SENSE)

OTP
CONFIGURATION

LDO2 (LP)
3.3 V OR 5.0 V @ 0.4 A

SELECTABLE WAKE-UP
WAKE PINS
GPIO (LP)
LDT
SPI

INTERNAL LDO REFERENCE
1.2 V/1.8 V/3.3 V/5.0 V

TRK1
INTERNAL LDO REFERENCE/
VREF/LDO2 @ 150 mA

VREF
3.3 V/5.0 V (±0.75 %)
@ 30 mA

TRK2
INTERNAL LDO REFERENCE/
VREF/LDO2 @ 150 mA

ISOLATION

VOLTAGE SUPERVISOR

WINDOW WATCHDOG
(SIMPLE/CHALLENGER)

LATENT FAULT CHECK
ABIST ON DEMAND

FIT FOR ASIL D
SAFETY LOGIC AND
CONTROL SPI,
INDEPENDENT
SAFETY MONITORING
UNIT

**S32 HW FAILURE
MONITOR (FCCU)**

OTP - iSMU

**IC HW
FAILURE MONITORING**

SAFETY OUTPUTS (RSTb, FS0b, FS1b)

aaa-045445

Figure 1. Functional block diagram

PB_FS26

Product brief

Rev. 2 — 1 June 2022

3 / 30

3 Features and benefits

Operating range

- 40 V DC maximum input voltage
- Support operating voltage range down to battery 3.2 V with VBST
- Support operating voltage range down to battery 6.0 V without VBST
- Low-power OFF mode with 30 μA quiescent current
- Low-power Standby mode with 25 μA quiescent current with VPRE active. LDO1 or LDO2 activation selectable via OTP configuration. GPIO1 or GPIO2 activation selectable via SPI communication.

Power supplies

- VPRE: synchronous buck converter with integrated FETs. Configurable output voltage and switching frequency, output DC current capability up to 1.5 A and PFM mode for Low-power Standby mode operation.
- VCORE: synchronous buck converter with integrated FETs. VCORE is dedicated for microcontroller core supply. Output DC current up to 0.8 A or 1.6 A (depending on part number), output voltage range setting from 0.8 V to 3.35 V.
- VBST: asynchronous boost controller with external low side switch, diode and current sense resistor. VBST is configurable as front-end supply to withstand low voltage cranking profiles or in back-end supply with configurable output voltage and scalable output DC current capability.
- LDO1: LDO regulator for microcontroller I/O support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- LDO2: LDO regulator for system peripheral support with selectable output voltage between 3.3 V and 5.0 V and up to 400 mA current capability.
- VREF: High precision reference voltage with 0.75 % accuracy for external ADC reference and internal tracking reference.
- TRK1 and TRK2: Voltage tracking regulators with selectable output voltage between VREF, LDO2 or Internal LDO reference. Support high-voltage protection for ECU off board operation. Each tracker has a current capability up to 150 mA.

System support

- Two wake-up inputs with high-voltage support for system robustness
- Two programmable GPIO with Wake-up capability or HS/LS driver
- Programmable Long Duration Timer (LDT) for system shutdown and wake-up control
- Monitoring of system voltages (including battery voltage monitoring) through the Analog Multiplexer
- Selectable wake-up sources from: WAKE/GPIO pins, LDT or SPI activity
- Device control via 32 bits SPI interface with Cyclic Redundancy Checks (CRC)

Compliance

- Electromagnetic Compatibility (EMC) optimization techniques for switching regulators, including spread spectrum, slew rate control and manual frequency tuning
- Electromagnetic Interference (EMI) robustness supporting various automotive EMI test standards

Functional Safety

- Scalable portfolio from Automotive Safety Integrity Levels (ASIL) B to D

- Independent monitoring circuitry, dedicated interface for microcontroller monitoring, simple and challenger watchdog function
- Analog Built-In Self-Test (ABIST) and Logical Built-In Self-Test (LBIST) at start-up
- Analog Built-In Self-Test (ABIST) on demand
- Safety outputs with latent fault detection mechanism (RSTB, FS0B, FS1B)

Configuration and enablement

- LQFP48 pins with exposed pad for optimized thermal management
- Permanent device customization via One-Time-Programming (OTP) fuse memory
- OTP emulation mode for system development and evaluation
- Debug mode for software development, MCU programming, and debugging

PB_FS26

Product brief

Rev. 2 — 1 June 2022

5 / 30

4 Applications

xEV and Powertrain market

- Inverter
- On-board charger (OBC)
- Battery Management System (BMS)
- Belt Starter Generator (BSG)

Body Market

- Gateway
- Zonal control
- Body Controller
- Smart Junction Box

Safety and Chassis

- Suspension
- Power Steering

MCU Attach

- NXP S32K3 family
- Infineon AURIX family (TC2xx and TC3xx)
- Renesas RH850 family
- Cypress Traveo family

5   Ordering information

This section describes the part numbers available for purchase, with their main differences. It also depicts how the part number reference is built.

5.1   Part number definition

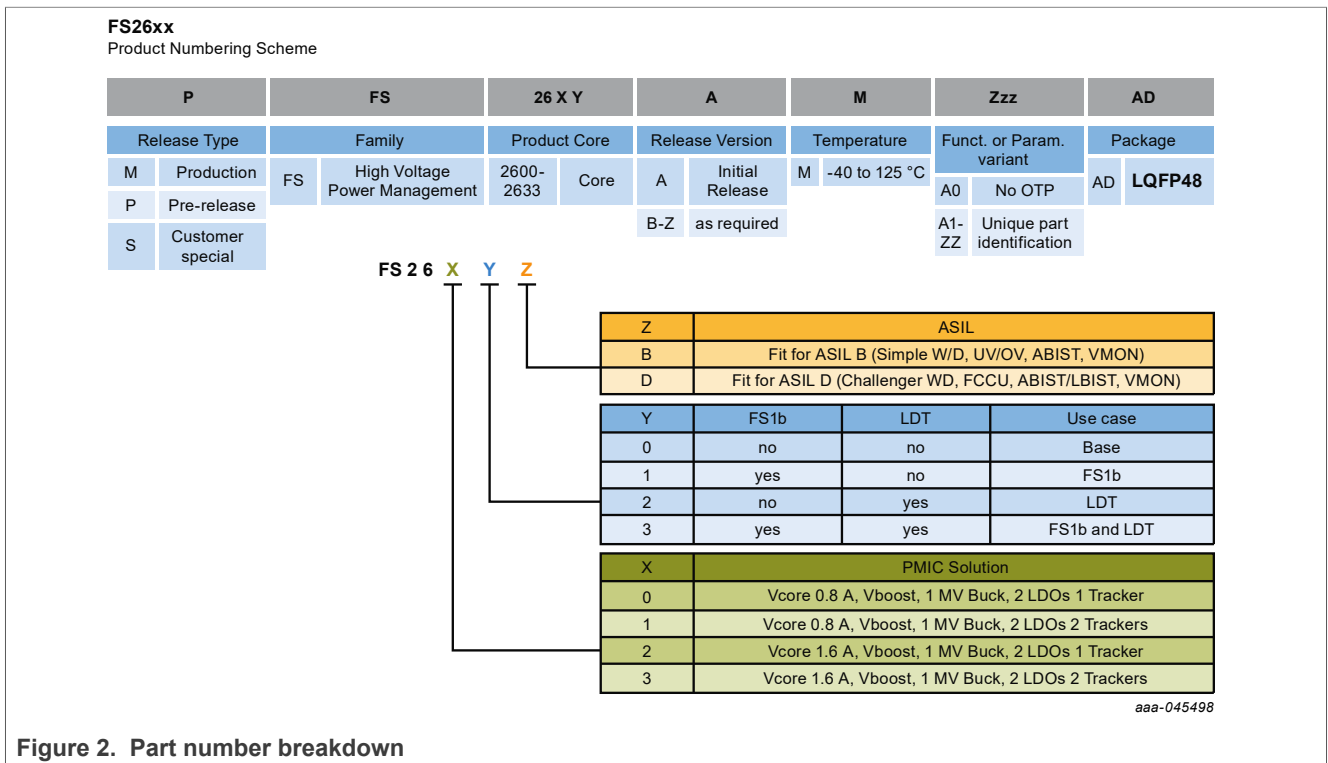Figure 2 shows how the FS26xyz part number is used to describe the available feature set of each device.

FS26xx
Product Numbering Scheme

P	FS	26 X Y	A	M	Zzz	AD
Release Type	Family	Product Core	Release Version	Temperature	Funct. or Param. variant	Package

Release Type			Family			Product Core			Release Version		Temperature		Funct. or Param. variant		Package	
M	Production		FS	High Voltage Power Management		2600-2633	Core		A	Initial Release	M	-40 to 125 °C	A0	No OTP	AD	**LQFP48**
P	Pre-release								B-Z	as required			A1-ZZ	Unique part identification		
S	Customer special															

FS 2 6 X Y Z

Z	ASIL
B	Fit for ASIL B (Simple W/D, UV/OV, ABIST, VMON)
D	Fit for ASIL D (Challenger WD, FCCU, ABIST/LBIST, VMON)

Y	FS1b	LDT	Use case
0	no	no	Base
1	yes	no	FS1b
2	no	yes	LDT
3	yes	yes	FS1b and LDT

X	PMIC Solution
0	Vcore 0.8 A, Vboost, 1 MV Buck, 2 LDOs 1 Tracker
1	Vcore 0.8 A, Vboost, 1 MV Buck, 2 LDOs 2 Trackers
2	Vcore 1.6 A, Vboost, 1 MV Buck, 2 LDOs 1 Tracker
3	Vcore 1.6 A, Vboost, 1 MV Buck, 2 LDOs 2 Trackers

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Figure 2. Part number breakdown

Figure 3 maps FS26 part numbers vs. product feature sets.

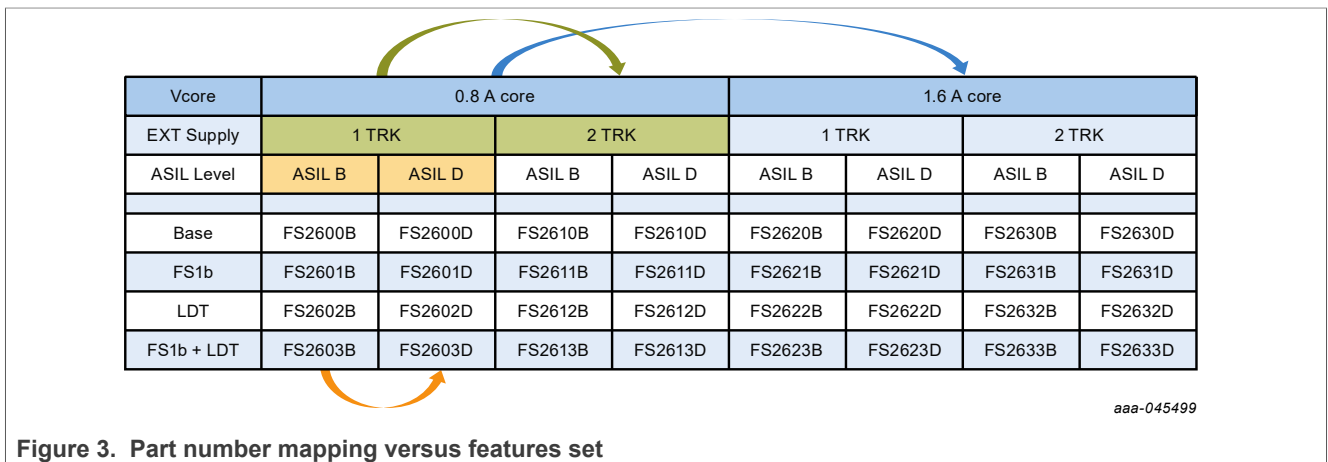| Vcore	0.8 A core				1.6 A core			
EXT Supply	1 TRK		2 TRK		1 TRK		2 TRK	
ASIL Level	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D	ASIL B	ASIL D
Base	FS2600B	FS2600D	FS2610B	FS2610D	FS2620B	FS2620D	FS2630B	FS2630D
FS1b	FS2601B	FS2601D	FS2611B	FS2611D	FS2621B	FS2621D	FS2631B	FS2631D
LDT	FS2602B	FS2602D	FS2612B	FS2612D	FS2622B	FS2622D	FS2632B	FS2632D
FS1b + LDT	FS2603B	FS2603D	FS2613B	FS2613D	FS2623B	FS2623D	FS2633B	FS2633D

aaa-045499

Figure 3. Part number mapping versus features set

5.2 Part number list

Table 1. Device segmentation

Part Number	DEV_ID	Tracker 2	Core Current Capability	Long Duration Timer	Tracker 2 Monitoring	FS1B	ABIST on demand	Watchdog Type	Fault Recovery	FCCU Monitoring	LBIST
FS2600B	0x01	NO	0.8 A	NO	NO	NO	YES	Simple	NO	Optional	NO
FS2601B	0x02	NO	0.8 A	NO	NO	YES	YES	Simple	NO	Optional	NO
FS2602B	0x03	NO	0.8 A	YES	NO	NO	YES	Simple	NO	Optional	NO
FS2603B	0x04	NO	0.8 A	YES	NO	YES	YES	Simple	NO	Optional	NO
FS2600D	0x05	NO	0.8 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2601D	0x06	NO	0.8 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2602D	0x07	NO	0.8 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2603D	0x08	NO	0.8 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2610B	0x09	YES	0.8 A	NO	YES	NO	YES	Simple	NO	Optional	NO
FS2611B	0x0A	YES	0.8 A	NO	YES	YES	YES	Simple	NO	Optional	NO
FS2612B	0x0B	YES	0.8 A	YES	YES	NO	YES	Simple	NO	Optional	NO
FS2613B	0x0C	YES	0.8 A	YES	YES	YES	YES	Simple	NO	Optional	NO
FS2610D	0x0D	YES	0.8 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2611D	0x0E	YES	0.8 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2612D	0x0F	YES	0.8 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2613D	0x10	YES	0.8 A	YES	YES	YES	YES	Challenger	YES	YES	YES
FS2620B	0x11	NO	1.6 A	NO	NO	NO	YES	Simple	NO	Optional	NO
FS2621B	0x12	NO	1.6 A	NO	NO	YES	YES	Simple	NO	Optional	NO
FS2622B	0x13	NO	1.6 A	YES	NO	NO	YES	Simple	NO	Optional	NO
FS2623B	0x14	NO	1.6 A	YES	NO	YES	YES	Simple	NO	Optional	NO
FS2620D	0x15	NO	1.6 A	NO	NO	NO	YES	Challenger	YES	YES	YES
FS2621D	0x16	NO	1.6 A	NO	NO	YES	YES	Challenger	YES	YES	YES
FS2622D	0x17	NO	1.6 A	YES	NO	NO	YES	Challenger	YES	YES	YES
FS2623D	0x18	NO	1.6 A	YES	NO	YES	YES	Challenger	YES	YES	YES
FS2630B	0x19	YES	1.6 A	NO	YES	NO	YES	Simple	NO	Optional	NO
FS2631B	0x1A	YES	1.6 A	NO	YES	YES	YES	Simple	NO	Optional	NO
FS2632B	0x1B	YES	1.6 A	YES	YES	NO	YES	Simple	NO	Optional	NO
FS2633B	0x1C	YES	1.6 A	YES	YES	YES	YES	Simple	NO	Optional	NO
FS2630D	0x1D	YES	1.6 A	NO	YES	NO	YES	Challenger	YES	YES	YES
FS2631D	0x1E	YES	1.6 A	NO	YES	YES	YES	Challenger	YES	YES	YES
FS2632D	0x1F	YES	1.6 A	YES	YES	NO	YES	Challenger	YES	YES	YES
FS2633D	0x20	YES	1.6 A	YES	YES	YES	YES	Challenger	YES	YES	YES

Additional part numbers will exist with different features and parametric settings. Table 1 is an example of a part number list.

Table 2. Orderable part numbers

PartNumber	Description	Package
MFS2613AMDA2AD	S32K3 + FS26 EVB ASIL D S32K3X4EVB-x257	LQFP48
MFS2613AMDA3AD	S32K344 HVBMS Reference design	
MFS2613AMDA4AD	S32K3 Body Control Module Reference design (white board)	
MFS2613AMDA6AD	S32K34448 V MC Development platform	
MFS2621AMDABAD	Aurix TC38, TC29	
MFS2613AMDDCAD	S32K3245G T-BOX + Gateway	
MFS2630AMDA0AD	Superset covering FS2630D devices	
MFS2630AMBA0AD	Superset covering FS2630B devices	
MFS2603AMBA0AD	Superset covering FS2603B devices	
MFS2603AMDA0AD	Superset covering FS2603D devices	
MFS2613AMBA0AD	Superset covering FS2613B devices	
MFS2613AMDA0AD	Superset covering FS2613D devices	
MFS2623AMBA0AD	Superset covering FS2623B devices	
MFS2623AMDA0AD	Superset covering FS2623D devices	
MFS2633AMBA0AD	Superset covering FS2633B devices	
MFS2633AMDA0AD	Superset covering FS2633D devices	

Empty OTP samples can be ordered for engineering purposes using part number **PFS2630AMDA0AD**. Refer to the associated OTP configuration report in the website product page.

6 Simplified application diagram

Figure 4 shows a simplified block diagram for a typical system with an FS26, using the boost controller to support battery cold-crank events.
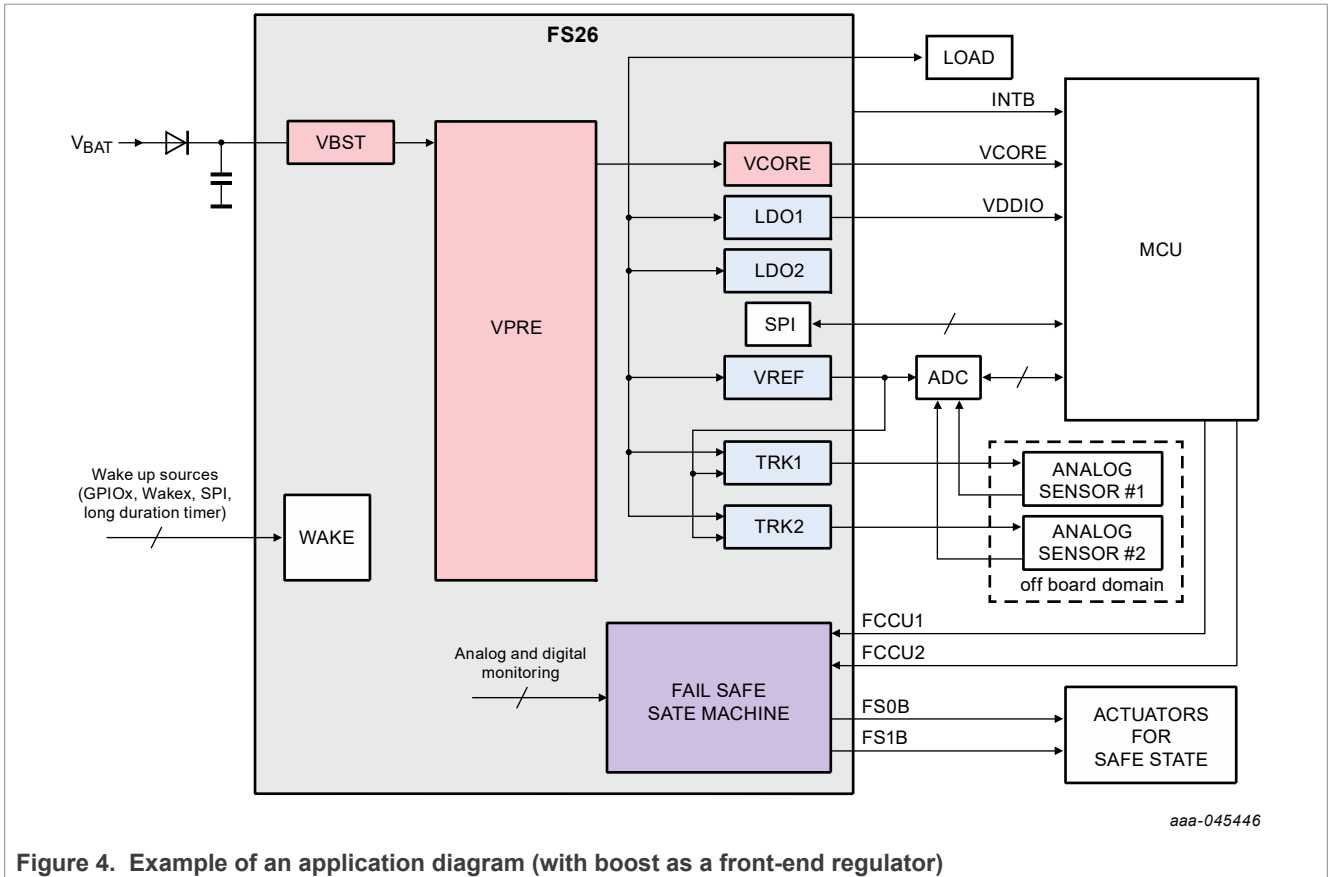
Figure 4. Example of an application diagram (with boost as a front-end regulator)

Figure 5 shows a simplified block diagram for a typical system with an FS26, using the boost controller to generate a voltage above the high voltage buck output voltage.

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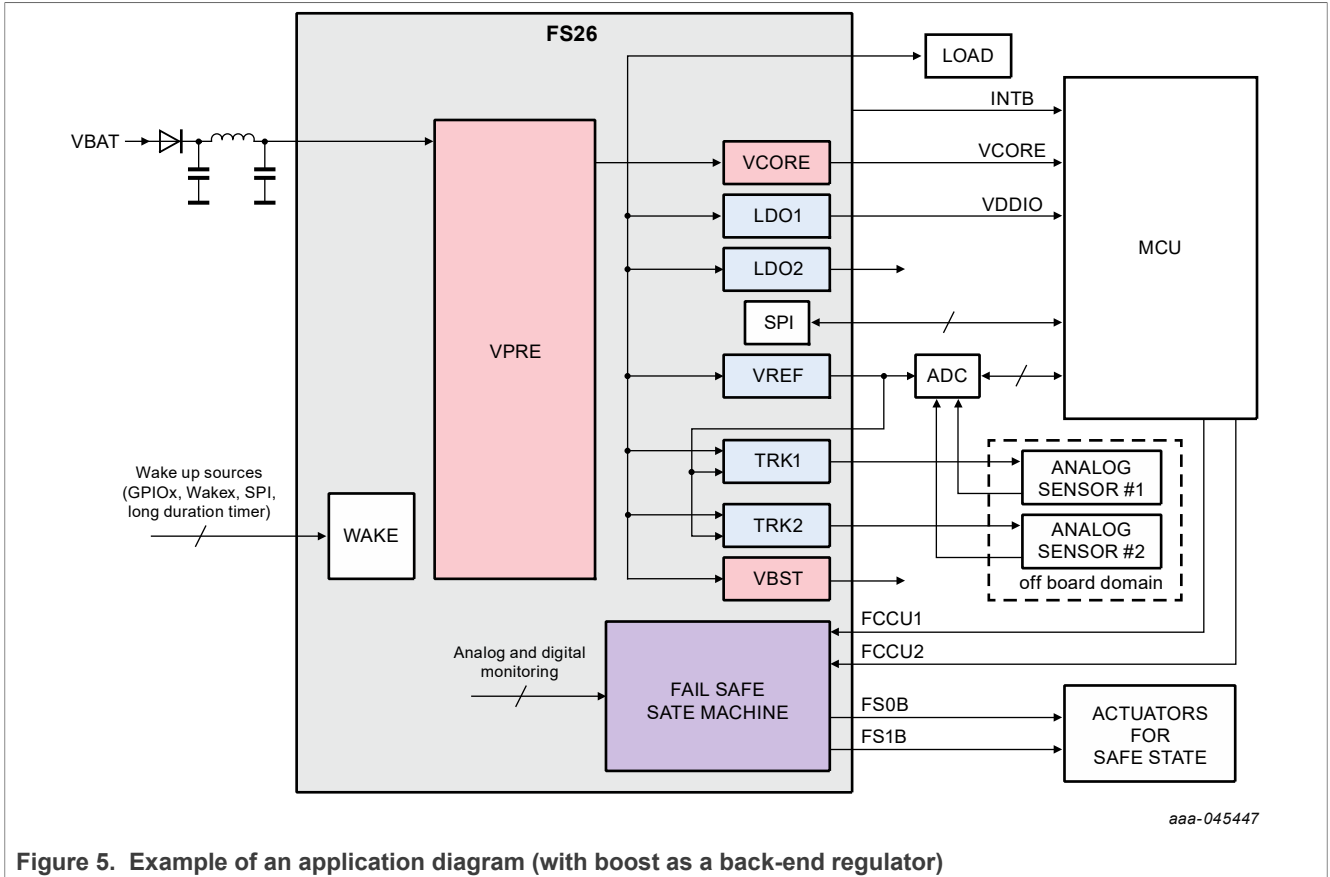
Figure 5. Example of an application diagram (with boost as a back-end regulator)

PB_FS26

Product brief

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Rev. 2 — 1 June 2022

11 / 30
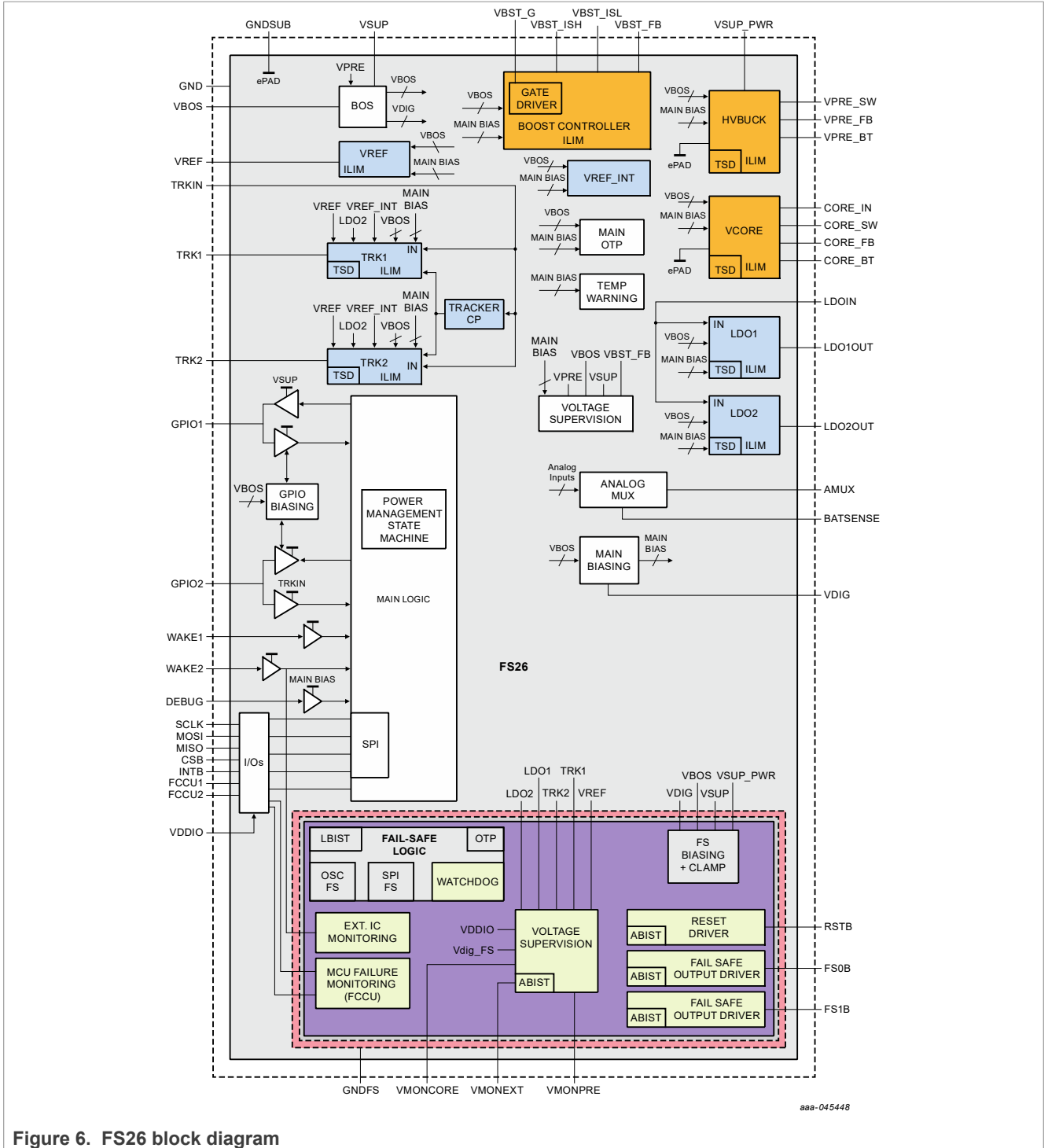
7 Block diagram

Figure 6. FS26 block diagram

PB_FS26

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Product brief

Rev. 2 — 1 June 2022

12 / 30

8 Pinning Information

8.1 Pinning

Figure 7. Pin assignment in LQFP48 package with exposed pad
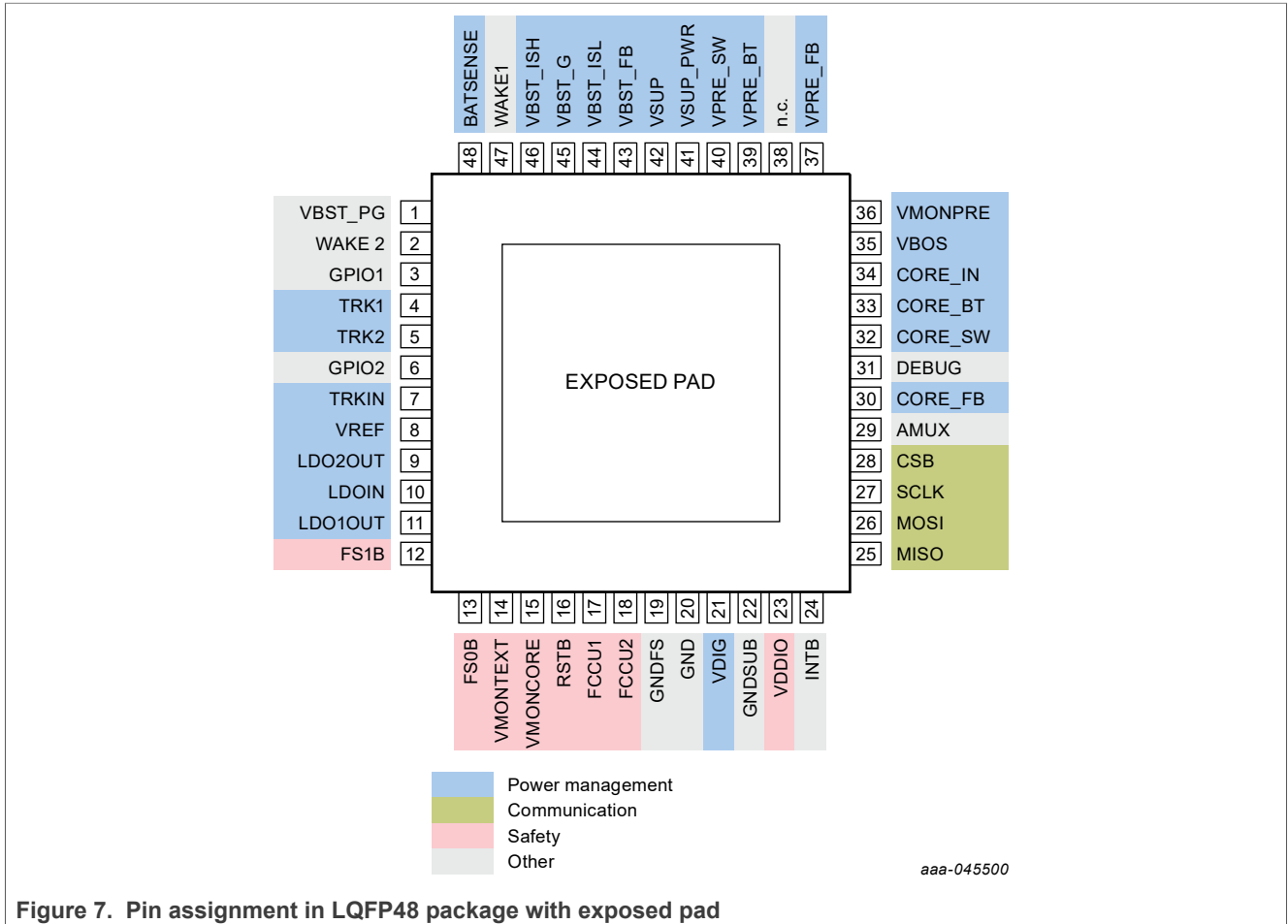
8.2 Pin descriptions

Table 3. Pin descriptions

Symbol	Pin number	Type	Description
VBST_PG	1	Digital output	Power Good signal for boost controller
WAKE2	2	Analog input	WAKE2 input pin or ERROR monitoring input
GPIO1	3	Analog output / Digital Input	General Purpose I/O 1
TRK1	4	Analog output	TRK1 output
TRK2	5	Analog output	TRK2 output
GPIO2	6	Analog output / Digital Input	General Purpose I/O 2
TRKIN	7	Analog input	Tracker Input
VREF	8	Analog output	Voltage refence output
LDO2OUT	9	Analog output	LDO2 output
LDOIN	10	Analog input	LDO input voltage supply
LDO1OUT	11	Analog output	LDO1 output
FS1B	12	Digital output	Safety output #1

Table 3. Pin descriptions...*continued*

Symbol	Pin number	Type	Description
FS0B	13	Digital output	Safety output #0
VMONEXT	14	Analog input	External voltage monitoring input
VMONCORE	15	Analog input	VCORE voltage monitoring input
RSTB	16	Digital output	Reset output
FCCU1	17	Digital input	Fault Control Collection Unit 1
FCCU2	18	Digital input	Fault Control Collection Unit 2
GNDFS	19	Ground connection	GND for fail-safe circuitry
GND	20	Ground connection	GND for main circuitry
VDIG	21	Analog output	1.6 V digital supply
GNDSUB	22	Ground connection	Substrate ground
VDDIO	23	Analog input	I/O input supply
INTB	24	Digital output	Interrupt output
MISO	25	Digital output	SPI Primary In Secondary out
MOSI	26	Digital input	SPI Primary Out Secondary input
SCLK	27	Digital input	SPI clock input
CSB	28	Digital input	SPI chip select
AMUX	29	Analog output	Analog Multiplexer output
CORE_FB	30	Analog input	VCORE feedback node
DEBUG	31	Digital input	DEBUG input pin
CORE_SW	32	Analog output	VCORE switching node
CORE_BT	33	Analog input	VCORE bootstrap supply
CORE_IN	34	Analog input	VCORE input supply
VBOS	35	Analog output	Best Of Supply decoupling output
VMON_PRE	36	Analog input	VPRE monitoring pin
VPRE_FB	37	Analog input	VPRE feedback node
NC	38	Not connected pin	Not connected pin
VPRE_BT	39	Analog output	VPRE boot strap capacitor
VPRE_SW	40	Analog output	VPRE switching node
VSUP_PWR	41	Analog input	VPRE converter supply pin
VSUP	42	Analog input	Supply pin for internal biasing
VBST_FB	43	Analog input	VBST feedback node
VBST_ISL	44	Analog input	VBST current sense low
VBST_G	45	Analog output	VBST low-side gate drive
VBST_ISH	46	Analog input	VBST current sense high
WAKE1	47	Analog input	WAKE1 input pin
BATSENSE	48	Analog input	Battery sense terminal
EP	49	Ground connection	Exposed pad (to be connected to GND)

PB_FS26

Product brief

Rev. 2 — 1 June 2022

14 / 30

9   Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
Voltage ratings				
VPRE_BT	DC voltage at VPRE_BT pin	-0.3	45.5	V
GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB	DC voltage at GPIO1, GPIO2, FS1B, FS0B, VMONEXT, VMONCORE, VMONPRE, WAKE1, WAKE2, VPRE_SW, VBST_FB pins	-0.3	40	V
BATSENSE	DC voltage at BATSENSE pin with -10 mA maximum reverse current (recommended 5.1 kΩ serial resistor)	-18.0	40	V
TRK1, TRK2, VSUP, VSUP_PWR	DC voltage at TRK1, TRK2, VSUP_PWR, VSUP pins	-1.2	40	V
CORE_BT	DC voltage at CORE_BT pin	-0.3	12.5	V
DEBUG	DC voltage at DEBUG pin	-0.3	10	V
TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW	DC voltage at TRKIN, LDOIN, CORE_IN, VPRE_FB, CORE_SW pins	-0.3	7	V
VBOS	DC voltage at VBOS pin	-0.3	5.6	V
VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G, VBST_PG	DC voltage at VREF, LDO2OUT, LDO1OUT, RSTB, FCCU1, FCCU2, VDDIO, INTB, MISO, MOSI, SCLK, CSB, AMUX, CORE_FB, VBST_ISH, VBST_ISL, VBST_G and VBST_PG pins	-0.3	5.5	V
VDIG	DC voltage at VDIG pin	-0.3	2	V
GNDFS, GND, GNDSUB, EPAD	DC voltage at GNDFS, GND, GNDSUB pins and Exposed PAD (EPAD)	-0.3	0.3	V
WAKE1, WAKE2, GPIO1, GPIO2	DC maximum reverse current at WAKE1, WAKE2, GPIO1, GPIO2 pins	-5	—	mA

10 Electrostatic discharge

Table 5. ESD

Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (Rating)	Min	Max	Unit
ESD ratings				
Human body model: AEC-Q-100 Rev H.				
V_{ESD_HBM}	All pins	-2.0	2.0	kV
Charged device model: AEC-Q-100 Rev H				
V_{ESD_CDM1}	All pins	-500	500	V
V_{ESD_CDM2}	Corner pins	-750	750	V
Gun Test				
V_{ESD_CDT1}	ESD - GUN discharged contact test 330 Ω/150 pF unpowered according to IEC61000-4-2 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT2}	ESD - GUN discharged contact test 2 kΩ/150 pF unpowered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT3}	ESD - GUN discharged contact test 2 kΩ/330 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT4}	ESD - GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (VSUP_PWR, VSUP, FS0B, FS1B, TRK1, TRK2, GPIO1, GPIO2, WAKE1, WAKE2)	-8	8	kV
V_{ESD_CDT5}	Operating ESD- GUN discharged contact test 330 Ω/150 pF powered according to ISO10605.2008 Global pins (GND, BATSENSE, FS0B, FS1B). Criteria: CLASS A	-8	8	kV

11 Thermal ratings

Table 6. Temperatures ranges

Symbol	Description	Min	Typ	Max	Unit
T_A	Ambient temperature	-40	—	125	°C
T_J	Junction temperature	-40	—	150	°C
T_{STG}	Storage temperature	-55	—	150	°C
T_{WARN}	Temperature warning threshold to set TWARN_S SPI bit	145	155	170	°C

Table 7. Thermal resistance (per JEDEC JESD51-2)

Symbol	Description	Value	Unit
$R_{\theta JA}$	Thermal resistance Junction to Ambient [1]	25	°C/W
$R_{\theta JCBOTTOM}$	Thermal resistance Junction to Case Bottom (with uniformed power on the silicon die)[2][3]	1.7	°C/W
$R_{\theta JCTOP}$	Thermal resistance Junction to Case Top [3]	13.5	°C/W
Ψ_{JT}	Thermal characterization parameter Junction to Top [4] [1]	0.8	°C/W

[1] Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
[2] Thermal resistance between the die and the printed circuit board. Board temperature is measured on the top surface of the board near the package.
[3] For exposed pad packages where the pad would be expected to be soldered, junction to case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance.
[4] Thermal test board meets JEDEC specification for this package (JESD51-7).

12 Packaging

12.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 8. Package mechanical dimensions

Package	Suffix	Package outline drawing number
7.0 × 7.0, 48–Pin LQFP exposed pad, with 0.5 mm pitch, and a 4.5 × 4.5 exposed pad	AE	98ASA00945D

12.2 Package outline

Figure 8. SOT1571-6

H-PQFP-G-48 I/O
7 X 7 X 1.5 PKG, 0.5 PITCH

SOT1571-6

DETAIL E
4X

44X 0.5

0.25

X X=A, B OR D

5.2 MAX
3.5 MIN

5.2 MAX

3.5 MIN

EXPOSED
PAD

VIEW F-F

9

DETAIL G

1.45
1.35

0.15
0.05

0.7
0.5

(1)

(0.15)

7:
0:

0.25

GAUGE
PLANE

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DATE: 30 MAR 2022

| MECHANICAL OUTLINE
PRINT VERSION NOT TO SCALE | STANDARD:
NON-JEDEC | DRAWING NUMBER:
98ASA00945D | REVISION:
B | PAGE:
2 |
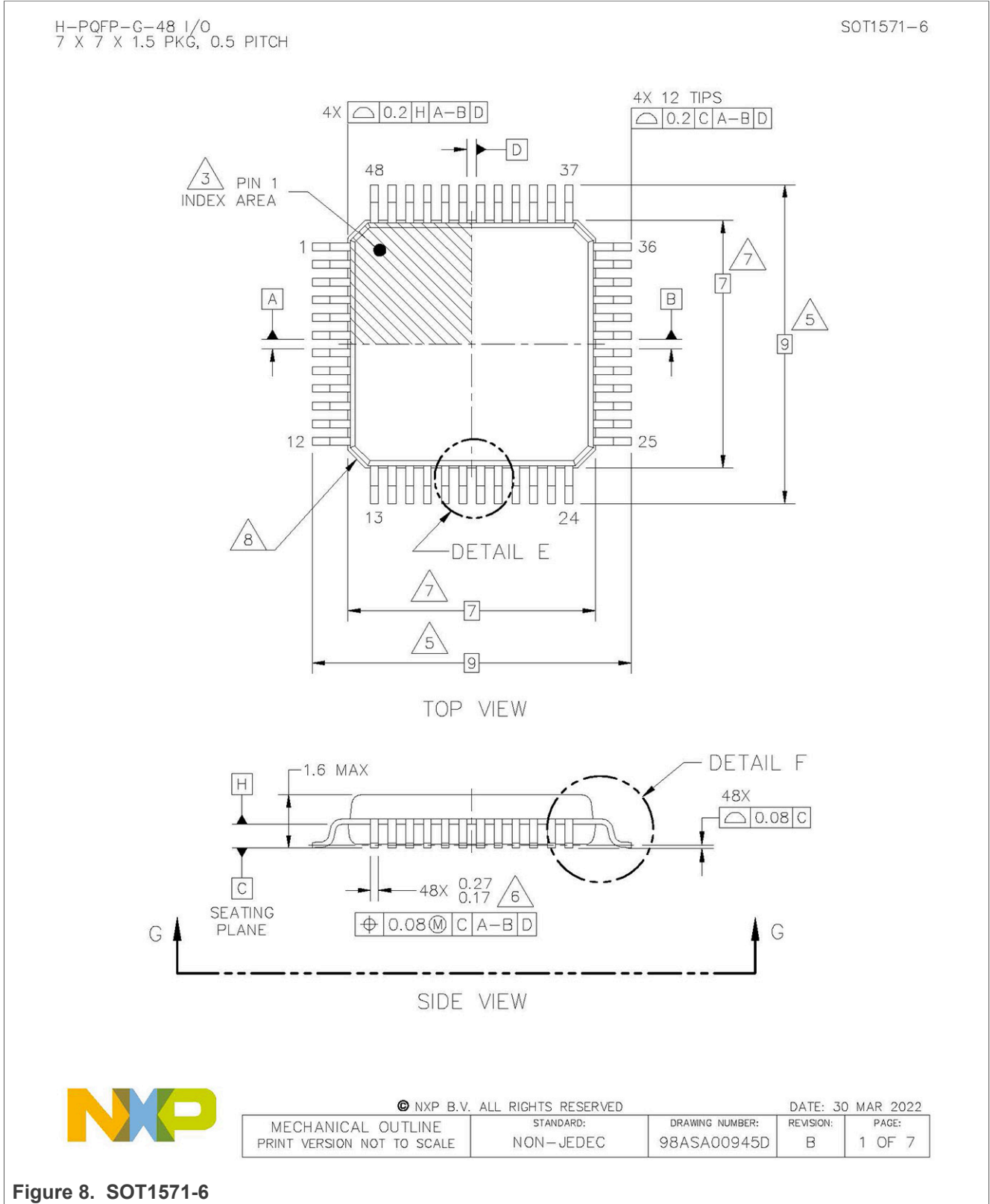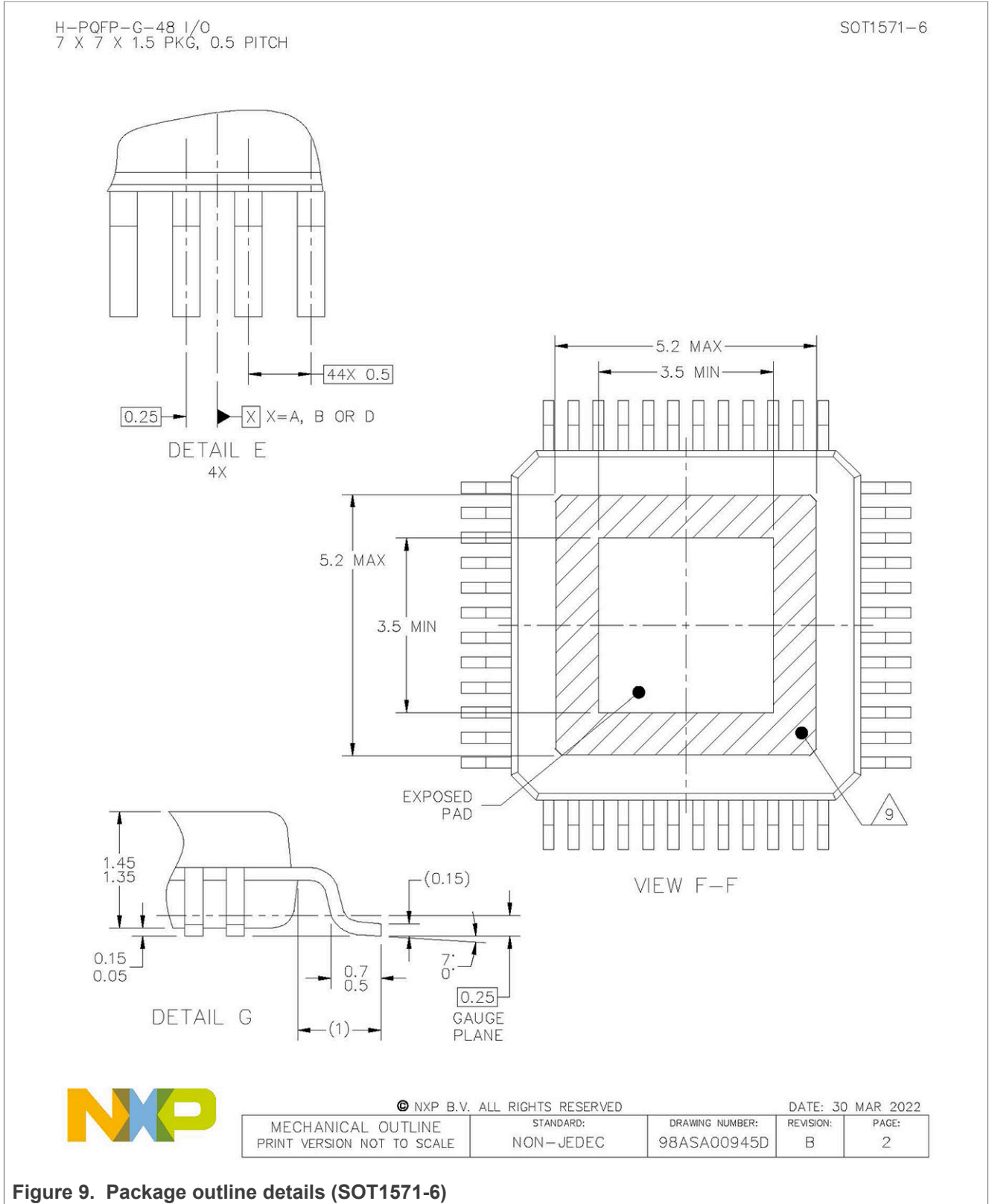
Figure 9. Package outline details (SOT1571-6)

PB_FS26

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Product brief **Rev. 2 — 1 June 2022**

20 / 30

H-PQFP-G-48 I/O   SOT1571-6
7 X 7 X 1.5 PKG, 0.5 PITCH

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.

3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.

4. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

5. DIMENSION TO BE DETERMINED AT SEATING PLANE C.

6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR
PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT
BY MORE THAN 0.08MM AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE
LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN
PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07MM.

7. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION
IS 0.25MM PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION
INCLUDING MOLD MISMATCH.

8. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

9. HATCHED AREA REPRESENTS POSSIBLE MOLD FLASH ON EXPOSED PAD.

10. KEEP OUT ZONE REPRESENTS AREA ON PCB THAT MUST NOT HAVE ANY EXPOSED METAL
(TRACE/VIA) FOR PCB ROUTING DUE TO THE POSSIBILITY OF SHORTING TO TIE
BAR/EXPOSED PAD.

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MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON−JEDEC	DRAWING NUMBER: 98ASA00945D	REVISION: B	PAGE: 6

Figure 10. Package outline notes (SOT1571-6)

H-PQFP-G-48 I/O
7 X 7 X 1.5 PKG, 0.5 PITCH

SOT1571-6

0.25

11X 0.5

(48X 0.37)

(48X 1.6)

0.25

11X 0.5

(4)

2X 4.25

PACKAGE
OUTLINE

(4)

2X 4.25

PCB DESIGN GUIDELINES — SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION.
DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING
PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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DATE: 30 MAR 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA00945D	REVISION: B	PAGE: 3

Figure 11. PCB design guidelines - solder mask opening pattern (SOT1571-6)

PB_FS26

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Product brief **Rev. 2 — 1 June 2022**

22 / 30
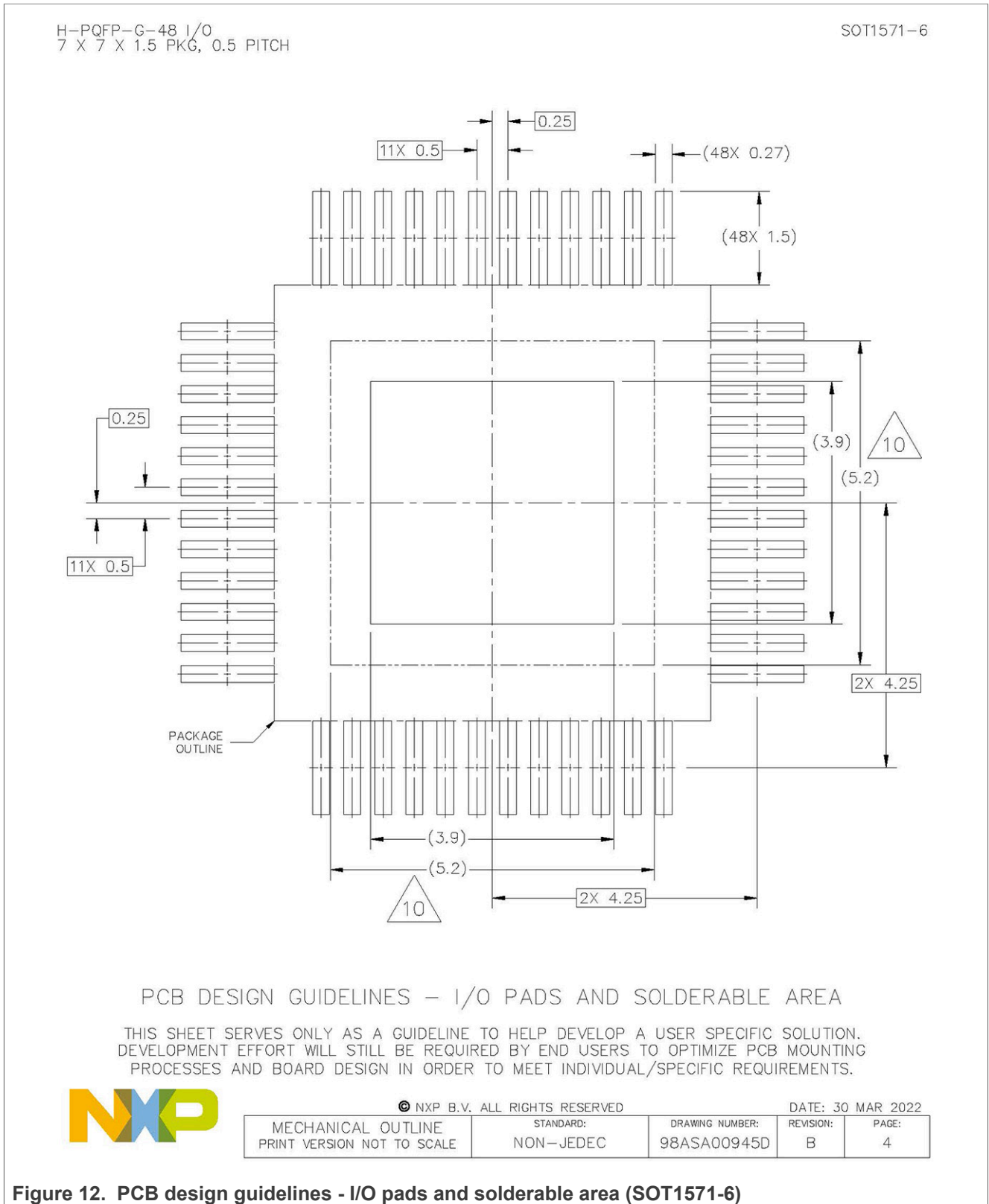
Figure 12. PCB design guidelines - I/O pads and solderable area (SOT1571-6)

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Product brief

Rev. 2 — 1 June 2022

23 / 30
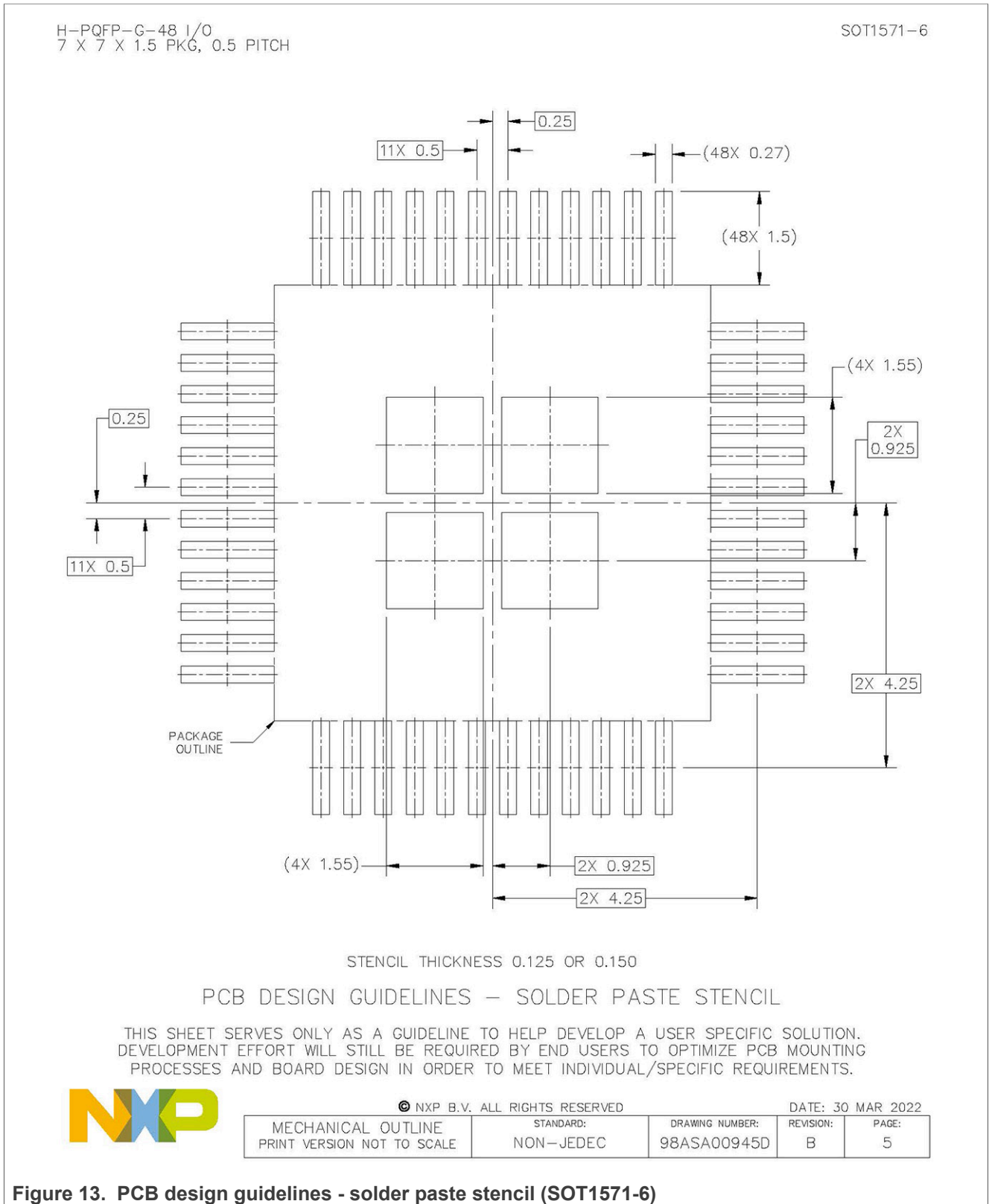
Figure 13. PCB design guidelines - solder paste stencil (SOT1571-6)

PB_FS26

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Product brief

Rev. 2 — 1 June 2022

24 / 30

13 References

Table 9. References

Documents, Tools, Enablement	URL
FS26 Functional Safety Manual	https://www.nxp.com/mynxp/secure-files
FS26 Dynamic FMEDA	https://www.nxp.com/mynxp/secure-files
AN12995 - FS26 Product Guidelines	https://www.nxp.com/mynxp/secure-files
FS26_SMPS_Calculator.xls	https://www.nxp.com/mynxp/secure-files
FS26 SMPS Simplis models	https://www.nxp.com/mynxp/secure-files
FS26 Graphical User Interface • To calculate the power dissipation • To create an OTP configuration • To interface an EVB KIT with a computer	https://www.nxp.com/mynxp/secure-files
FS26 Product Overview	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-sbc-with-low-power-fit-for-asil-d:FS26
KITFS26AEEVM: FS26 Evaluation Board	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/fs26-safety-sbc-evaluation-board:KITFS26AEEVM
KITFS26SKTEVM: FS26 Socket Board	https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/fs26-safety-sbc-programming-socket-board:KITFS26SKTEVM

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Product brief

Rev. 2 — 1 June 2022

26 / 30

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PB_FS26

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Product brief

Rev. 2 — 1 June 2022

27 / 30

Tables

Figures

PB_FS26

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Product brief

Rev. 2 — 1 June 2022

29 / 30

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