Layout Hints Application Note for TLE987x

Z8F68417618

Table of contents

1 Abstract

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This application note is intended to provide application hints when using TLE987x in a typical automotive 12V BLDC Motor Driver Application.

This application note must be used in conjunction with the latest TLE987x datasheet for a detailed component description. It is meant as an add-on to the datasheet and not as a document explaining the device in detail. It is also not a replacement to the datasheet.

This application note refers to the TLE9879QXA40 Datasheet Rev.1.0 from 02. February 2017.

2 Application circuit

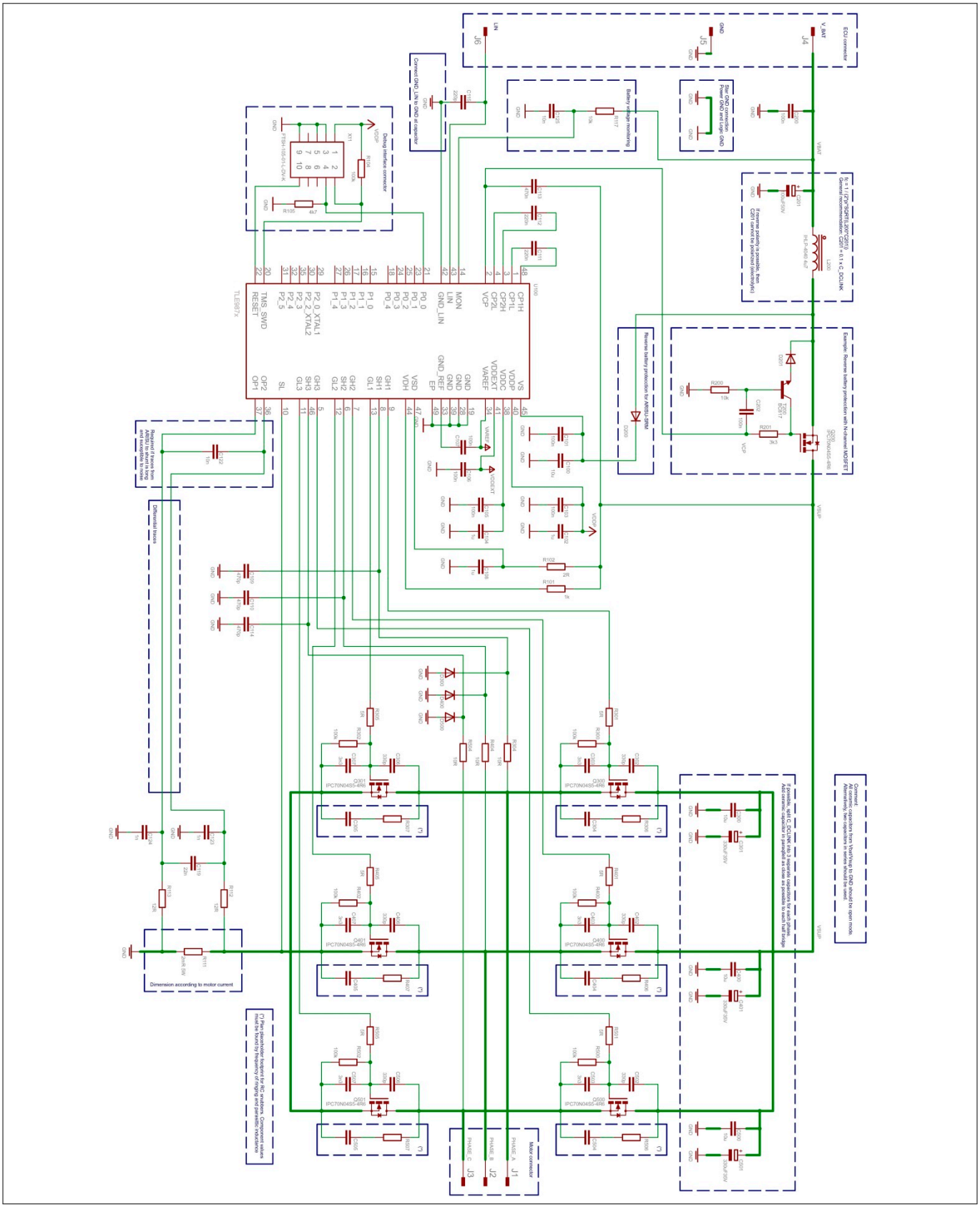


Figure 1 Simplified ECU circuit example

3 EME recommendation

There are some general recommendations for PCB layout as well as some specific items for microcontroller with bridge driver, like TLE987x.

3.1 Recommendations for optimized PCB layout

Electromagnetic emission (EME) is mainly radiated by the PCB and the attached cables. The cables are very efficient antennas especially for common mode currents. Loops on the PCB are regarded as good emitting antennas. Loops inside an IC are considered to be small compared to the external loops on PCB and cabling. EME from the IC can be neglected in most cases.

3.1.1 Placement of the connectors

Connectors on both sides of the PCB might cause high emission. A good PCB design would place the connectors on the same side.

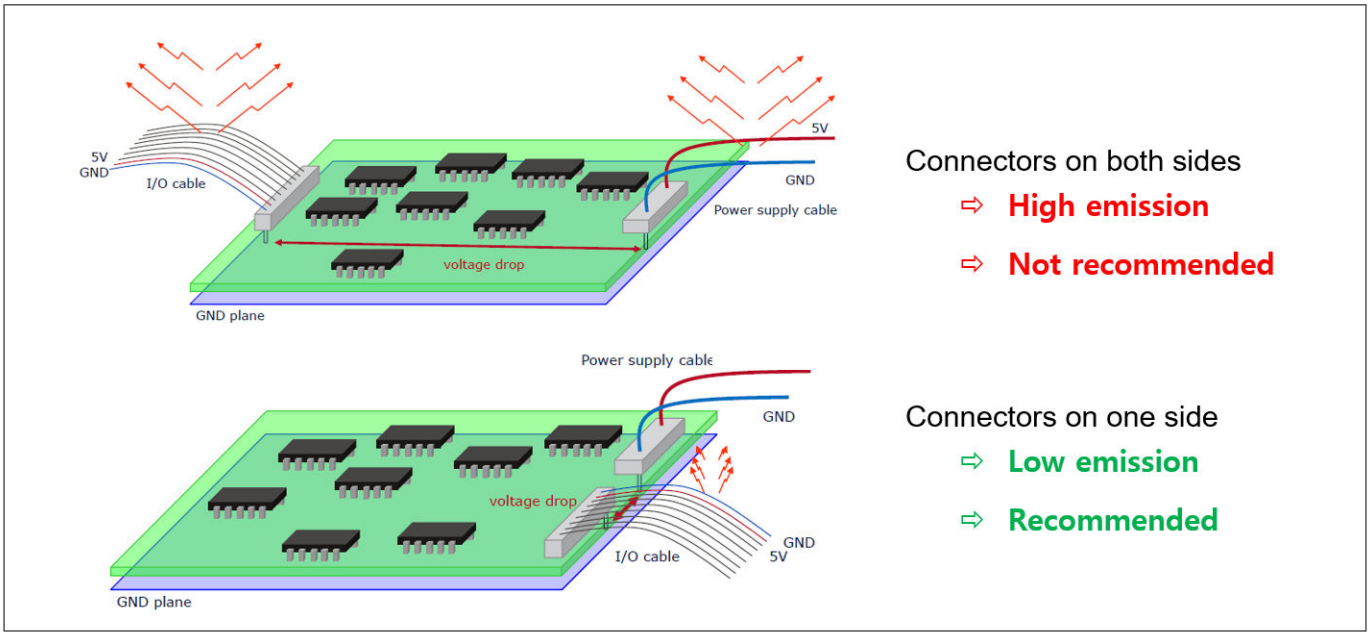


Figure 2 Placement of the connectors

3.1.2 Floor planning the PCB

For the components placement, following rules should be considered:

All components from one group should be located together (power, digital, analog, supply, …)

Connectors only on one side

Susceptible parts away from noisy parts (power, digital, analog)

Parts that generate noise should be close to the connector

Route all traces to the components in each zone as if this zone would have its own Ground plane

Number the components in each zone in the same way (e.g. Analog = 100, Digital = 200, Power = 300,…)

3.1.3 Routing of the power supply traces

Wiring loops on the PCB should be as small as possible.

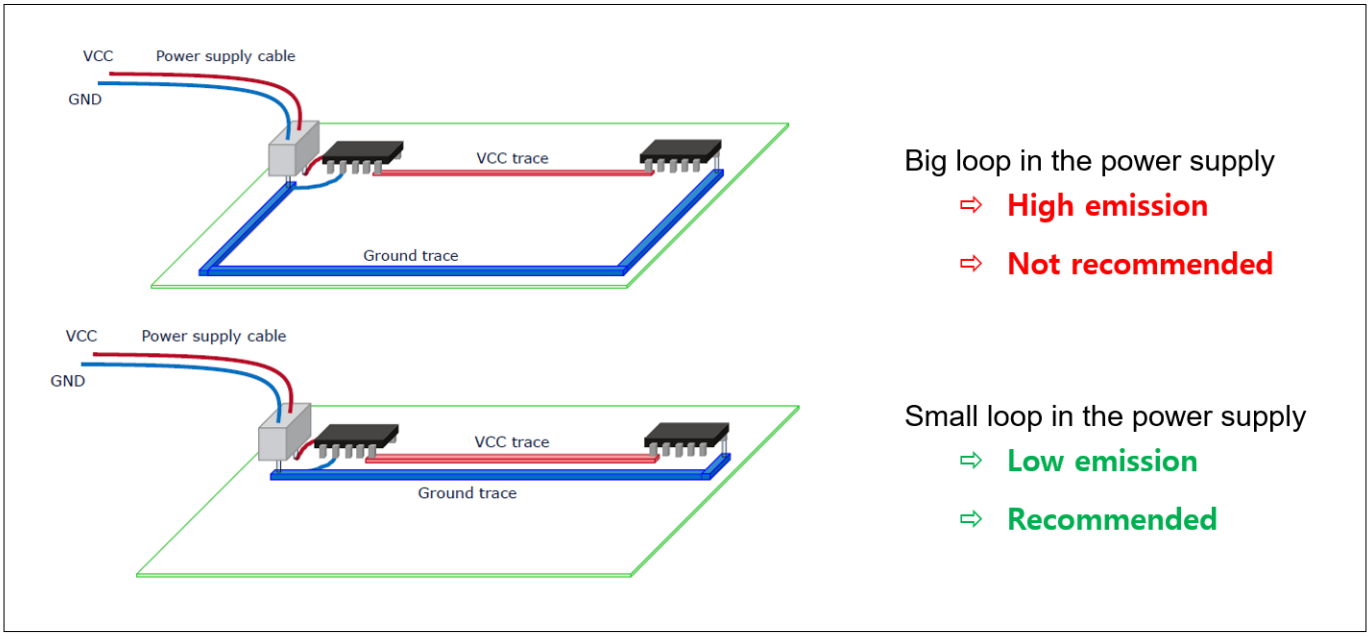
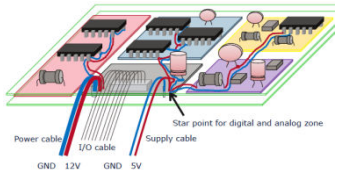
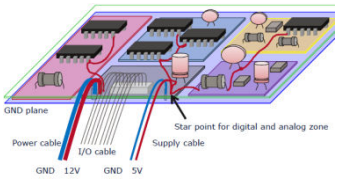
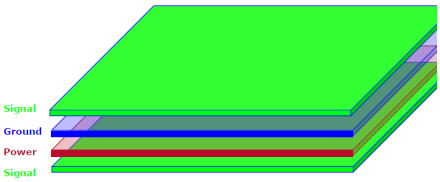
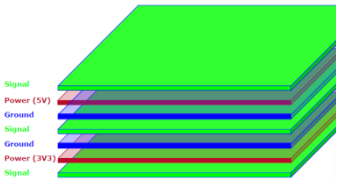


Figure 3 Routing of the power supply

3.1.4 Number of PCB layers

Table 1 Rules for different PCB types

Two layer PCB (no Ground plane)		• Keep the loop areas that are formed by Ground and Power supply traces as small as possible • Route Power supply traces always together (parallel, next to each other) starting from once central start point and spreading into each individual zone • Do not mix the supplies of different zones • Fill free areas with Ground
Two layer PCB (solid Ground plane)		• Use a solid Ground plane • Components of one zone should be supplied by only one supply from a central star point • Do not mix supply of different zones • No loops are allowed for supply traces (tree structure)
Multi layer configuration (4 layers)		• Keep Ground and Power supply layers next to each other => provides a good decoupling capacitor for free • Avoid slots in Ground and Power supply planes (e.g. by routing signal traces within these planes, vias in a row, through hole connectors,…)
Multi layer configuration (> 4 layers)		• Route critical signals (e.g. high frequency signals, susceptible signals) in an inner signal layer that is embedded by two Ground layers • Give each power supply domain (e.g. 5V, 3.3V, …) a separate Power and Ground plane

4 Specific PCB design rules for microcontroller with bridge driver

Some general recommendations:

- Separate the IC supply (VS and VSD) from VDH, i.e. separate voltage sense line from power stage.
- Due to observed power dissipation during transient tests, recommended package for serial resistor at MON is SMD1206.
- Placeholder for RC snubber circuit for all bridge MOSFET shall be considered for damping of circuit resonances during switching (if needed).
- For better filter performance and life time, low ESR electrolytic capacitors, rated for higher ripple current, shall be used.
- If using sense resistor, the maximum allowed capacitance between VDH and SL is < 30 uF (higher values would affect the current sensing too much).

4.1 Input filter

The Input Pi-filter is required for PWM application. The component values depend on switching frequency and motor current (***Figure 4***).

The best value of filter capacitor C13 is 1/10 of the input capacitor C15, to optimize the filter performance. In case, that a electrolytic capacitor cannot be used for C13 due to reverse polarity requirement, a ceramic capacitor with a value >10 uF would be an alternative.

GND connection of C13 should be the common GND star point (use ground plane)

In order to avoid RF disturbances entering the board from outside, ceramic capacitor C14 should be placed as close as possible to the ECU connector.

C16 is optional and shall be used in case of a floating motor case, to force the common mode current back to the source.

The input capacitor C15 is an alternative in case of space limitation for three single capacitors. A much better solution are three capacitors placed close to each phase to reduce the loop of the commutation circuit (C28, C48, C68 in C48). Each of this capacitors should have a value of ~ 330 uF with low ESR value.

For IC input filters (D1, C1 and C2), separation of IC and MOSFET power current enables more efficient filtering.

C1 value is recommended to use > 47 uF.

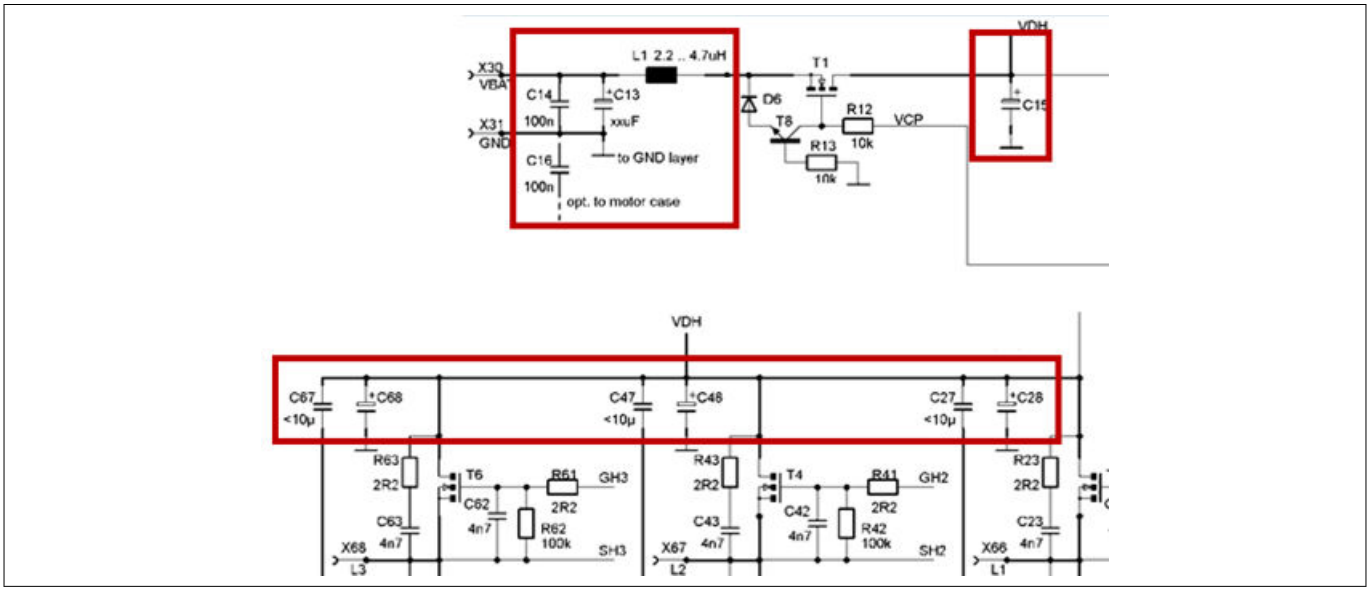


Figure 4 Input Pi-filter and Input capacitor

4.2 GND concept

The general suggestion for pouring the ground planes in a TLE987x project is to keep as much as possible the power MOSFETs' switching currents and the IC operation currents separated. In ***Figure 5*** the reader can clearly distinguish these currents as well as the different symbols used for their returning paths, that from now on we will call IC GND and PWR GND.

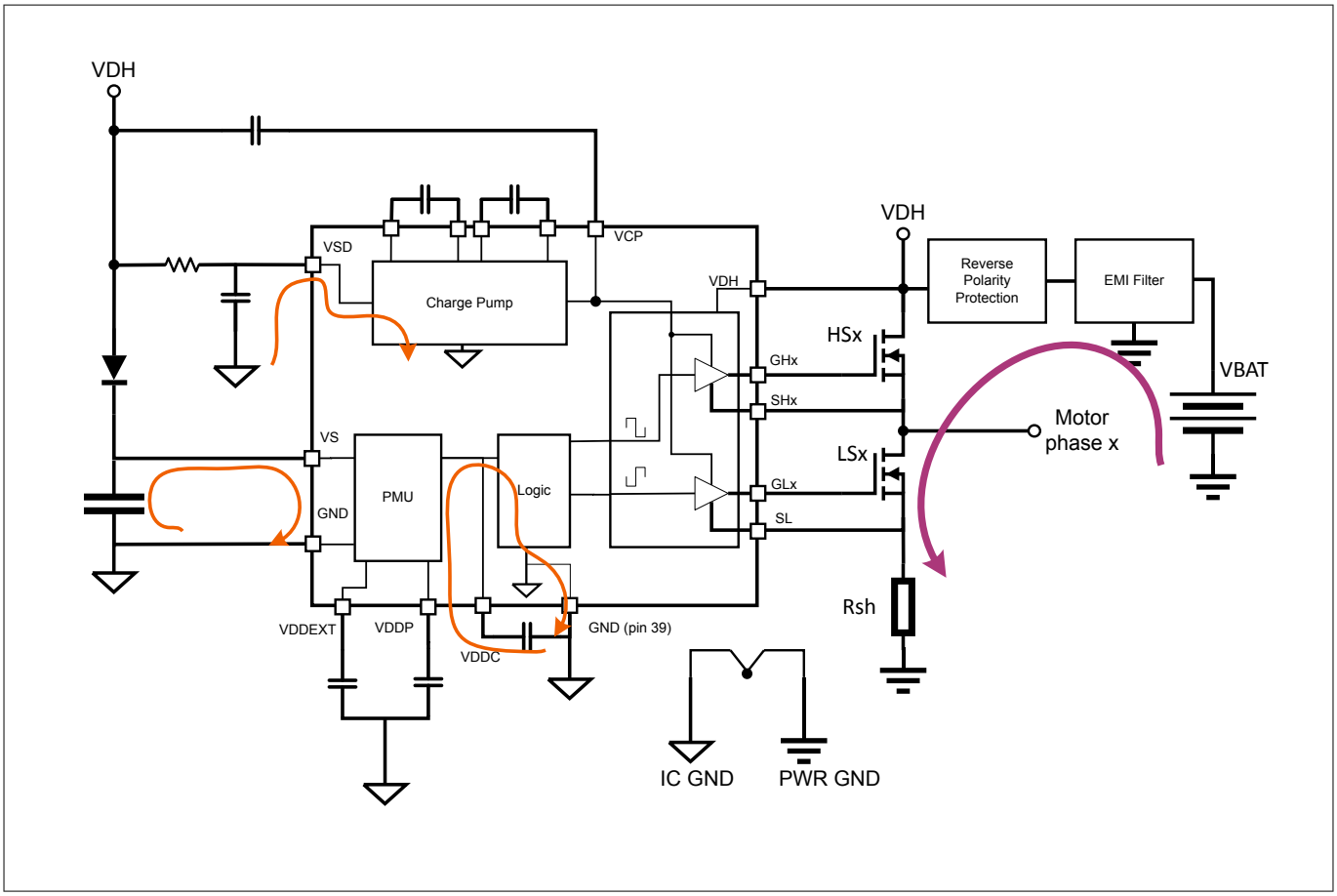


Figure 5 GND concept and main current paths: PWM switching currents in purple, IC supplies current in orange

This simple but effective schematization has two beneficial effects:

- prevents the three main GND pins, pin 39, 19 and 28, to be influenced by the PWM currents. In this way the internal ground connections of the analog and digital circuitry in the IC will be subject to limited voltage differences.
- high frequency currents interactions with the battery ground terminal will be limited.

A practical example is illustrated in ***Figure 6***. In particular, notice that the connection between PWR GND (Mid-top) and IC GND (Mid-bottom) planes consists of a slim trace and a via. This apparently weak connection actually ensures the IC's supply currents path while rejecting high frequency currents that could loop from the IC to the battery.

The GND pins routing of the IC should respect the following rules:

- Pin 39 should have the most solid connection to the IC GND plane. In the layout example this is accomplished by taking advantage of the exposed pad solid connection through multiple vias. Whenever this is not feasible, connect the VDDC capacitor's GND pin to IC GND with as many vias as possible.
- Pin 19 and 28 can exhibit a weaker connection to IC GND.

To minimize the stray inductance, the loop "input cap – bridge MOSFET – sense resistor" should be as small as possible.

4 Specific PCB design rules for microcontroller with bridge driver

To reduce digital GND bounce transmitted via LIN, GND_LIN shall not be connected directly to IC GND. It is better to have a slight decoupling by using few mm trace.

A typical conducted EMI spectrum of an application that follows these rules is shown in ***Figure 7***. In particular this measurement has been done on the layout example with the motor running functions turned off so to highlight the spectral contribution of the AC currents generated by the IC.

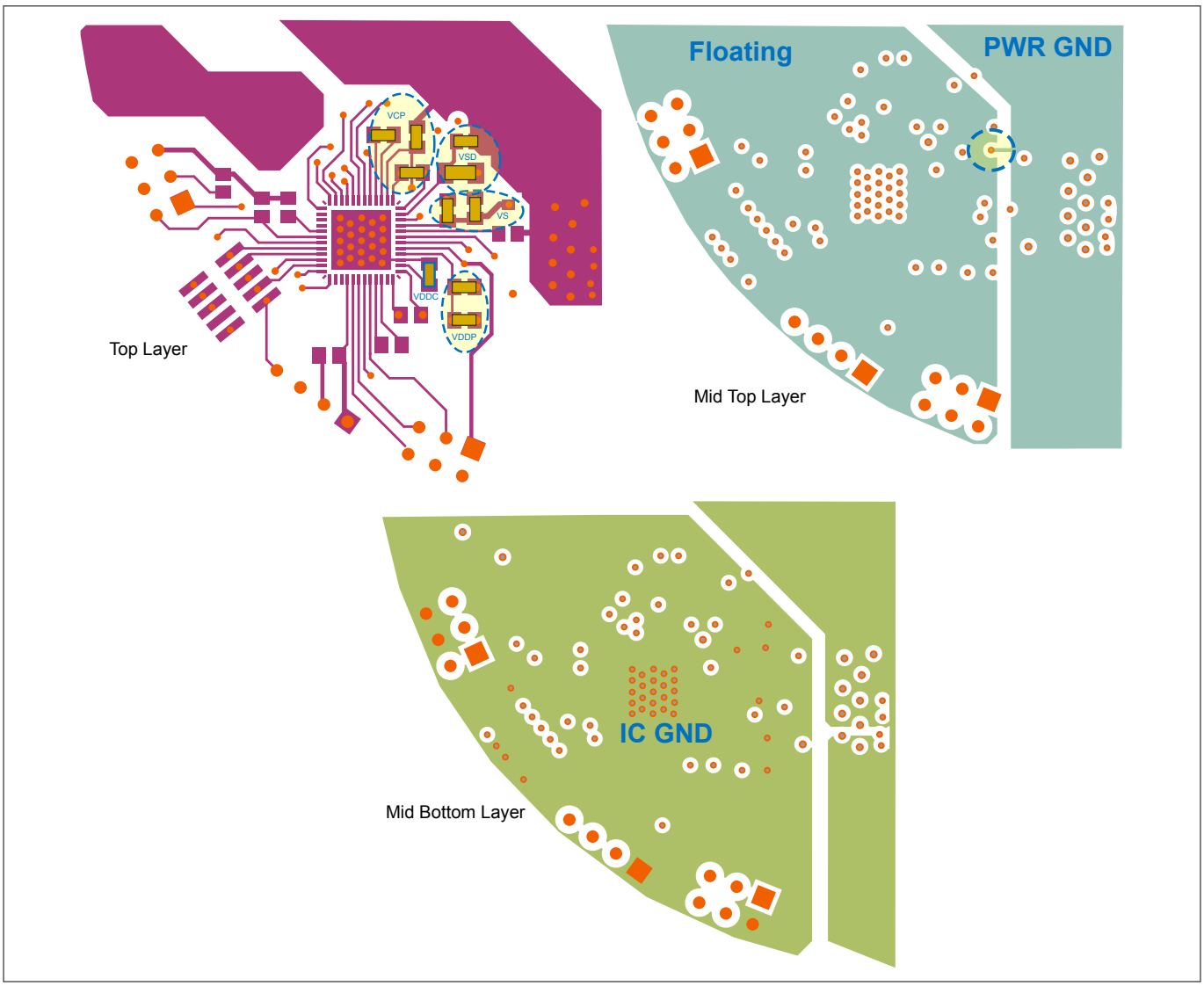


Figure 6 Example PCB Layers

4 Specific PCB design rules for microcontroller with bridge driver

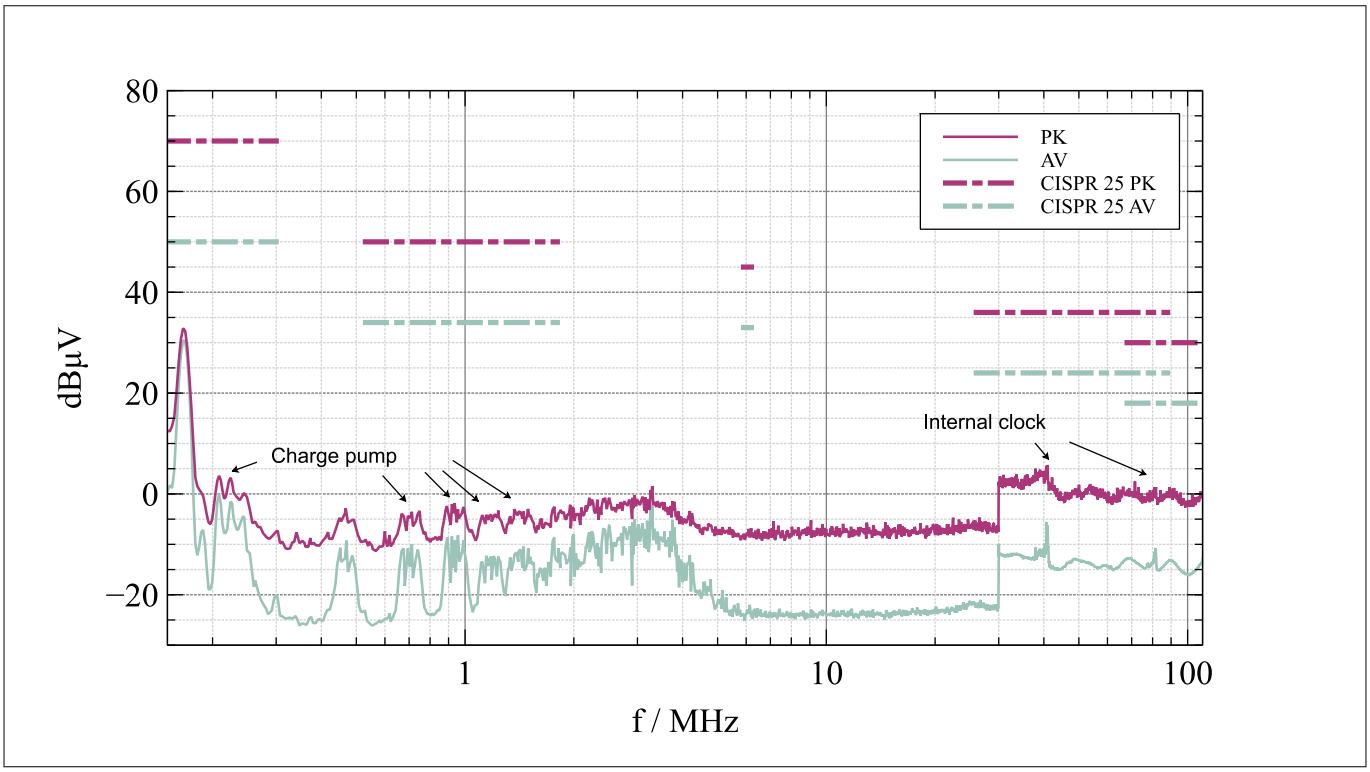


Figure 7 **Conducted EMI measurement spectrum related to the layout example**

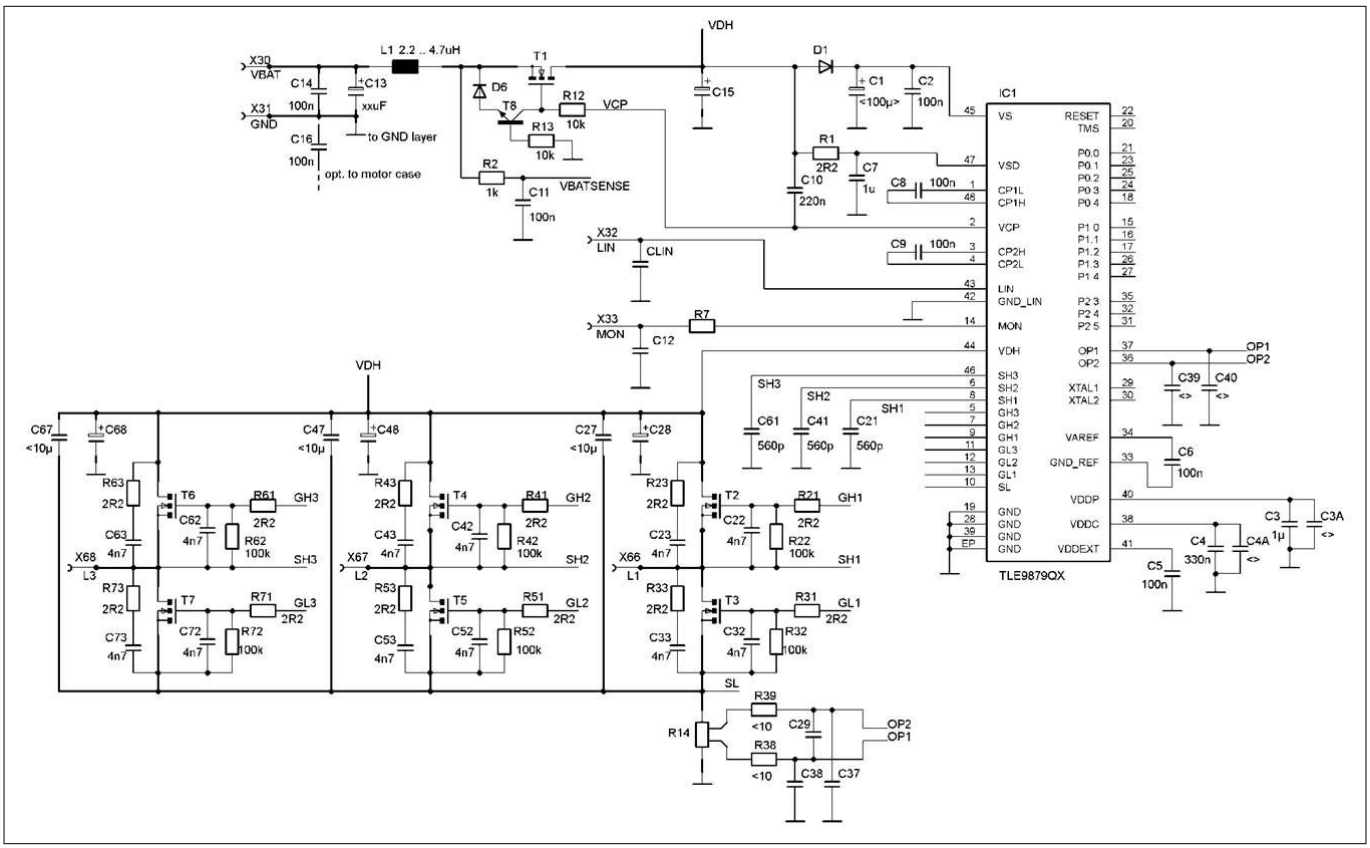


Figure 8 **Ground concept and blocking capacitors**

4.3 Blocking capacitors

Figure 8 is showing several blocking capacitors. Some comments and recommendations:

- For cost saving, most likely only one capacitor each at V_{DDC} and V_{DDP} is necessary.
- In order to keep the emitting or receiving loop as small as possible, C2 at VS and C4 at V_{DDC} should be placed as close as possible to the IC.
- In order to suppress RF disturbances entering the IC pin, additional capacitors with a value of 560 pF each should be placed at SHx close to the IC pin.
- C39 and C40 with a value < 10 nF are just placeholder for additional capacitors at OPx. Those are required if the distance to the sense resistor is higher than ~ 5 cm in order to suppress RF disturbances on this node coupled into the trace after R_{sense} filter.
- C6 shall only connect VAREF and GND_REF, no external GND connection. Shall be located as close as possible to the IC.
- In order to avoid RF disturbances traveling along the board before reaching the filter, all components around the sense resistor shall be placed as close as possible to the sense resistor. R38 and R39 with a value of ~10Ω, C37 and C38 with < 10 nF. C29 is just a placeholder for RF short for symmetry.
- In order to avoid reduce emitting loops, C8, C9 and C10 should be placed as close as possible to IC pin.

4.4 Layout recommendation for 3-phase motor bridge

Figure 9 is showing the commutation circuit of one bridge leg. This bridge leg can be a part of a two- or three-phase bridge.

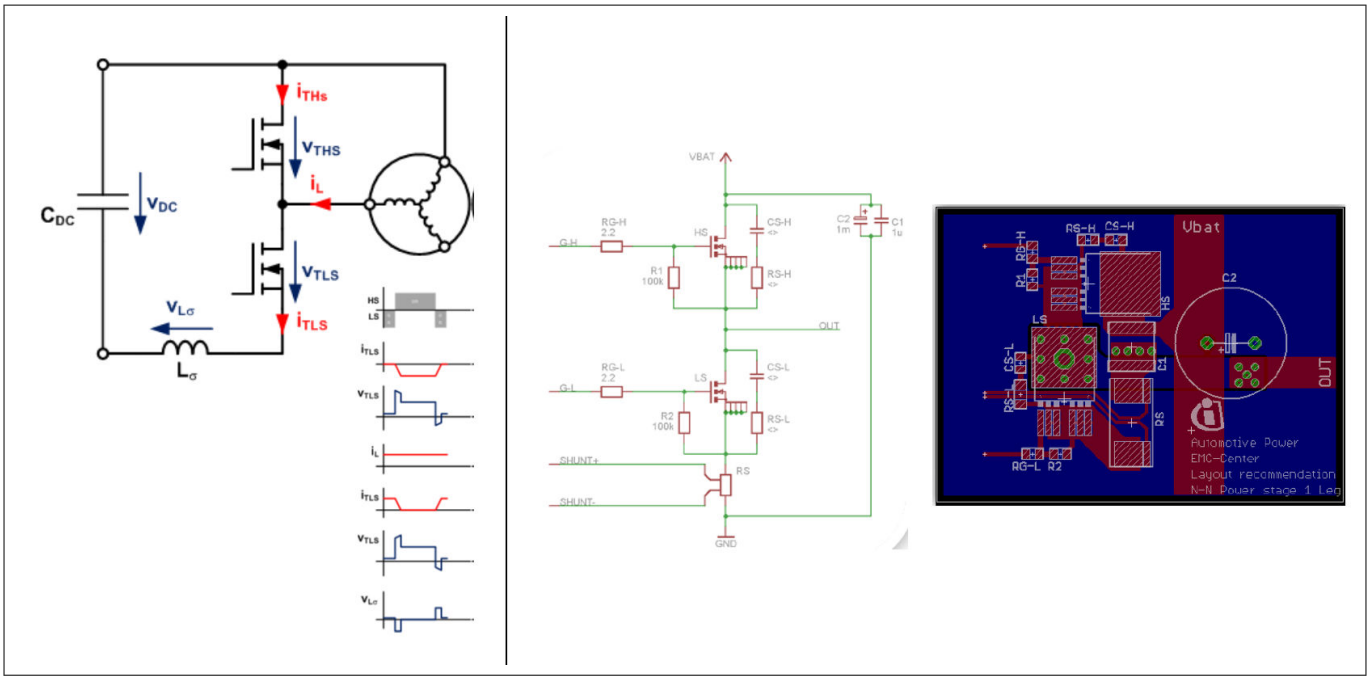


Figure 9 Layout – one bridge leg with two N-MOSFETs (as part of a 2- or 3-phase motor bridge)

During the switching from low-side to high-side the current is commutating from LS switch to HS switch. The ideal commutation circuit is the loop consisting of C_{DC}, T_{HS}, T_{LS}. The inductive part of the real circuit is considered in the stray inductance Lσ. Overvoltages are induced over Lσ during switching. These overvoltages are coupled direct to Out and to Vs and will also cause radiated emission. The size of the commutation circuit has to be as small as possible.

Figure 9 is also showing an example for a low impedance layout of one motor bridge leg. It can be seen that the capacitors C2, CS-H and CS-L are placed as close as possible to the device pins.

4 Specific PCB design rules for microcontroller with bridge driver

Figure 10 showing recommendation for the commutation circuit of 3-phase motor bridge.

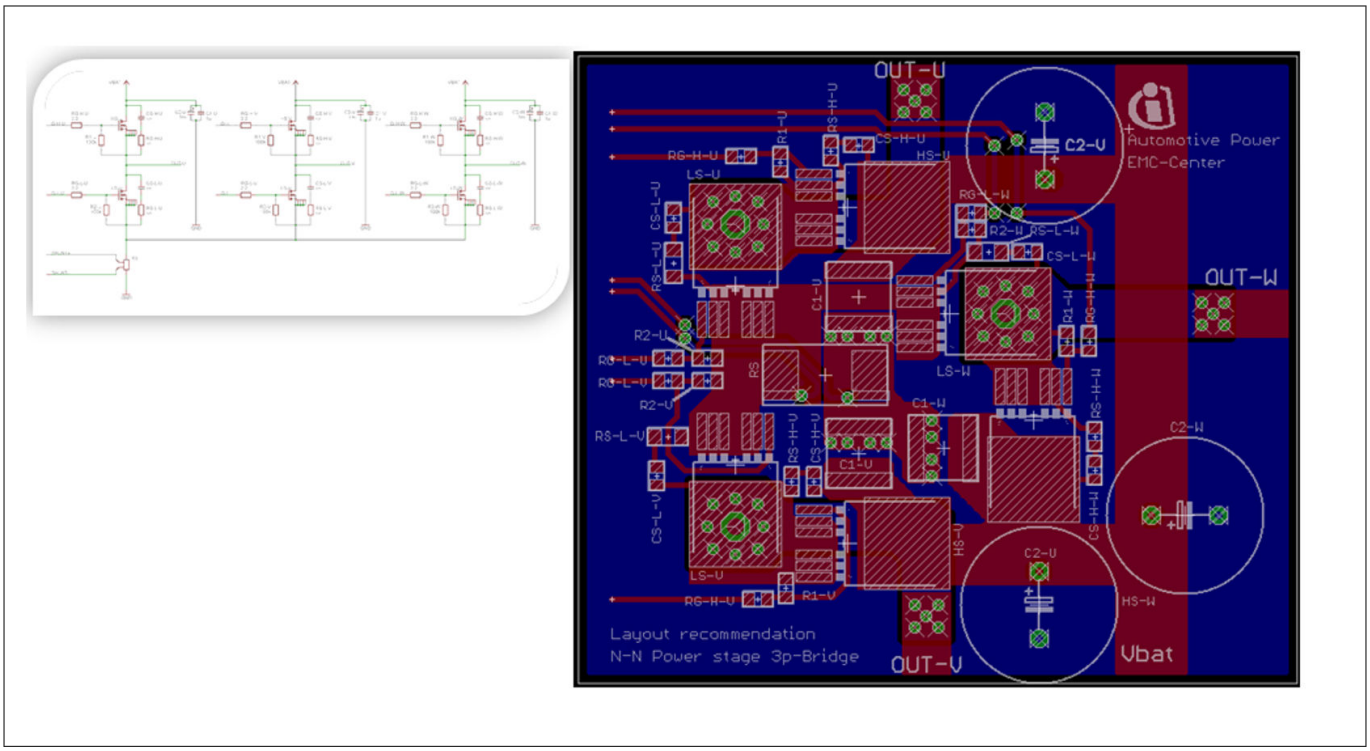


Figure 10 Layout recommendation – 3-phase motor bridge bridge

4.5 Layout recommendation for current sense shunt

Layout effects on current sensing shunts

A low inductive shunt is no guaranty for a low noise measurement signal

The quality of your signal depends on the layout with trace parasitics

- Use four wire sense approach with symmetric sense lines
- Avoid inductive coupling into the sense wires
- Take care of capacitive currents on the leads in presence of high dV/dt (common mode noise)

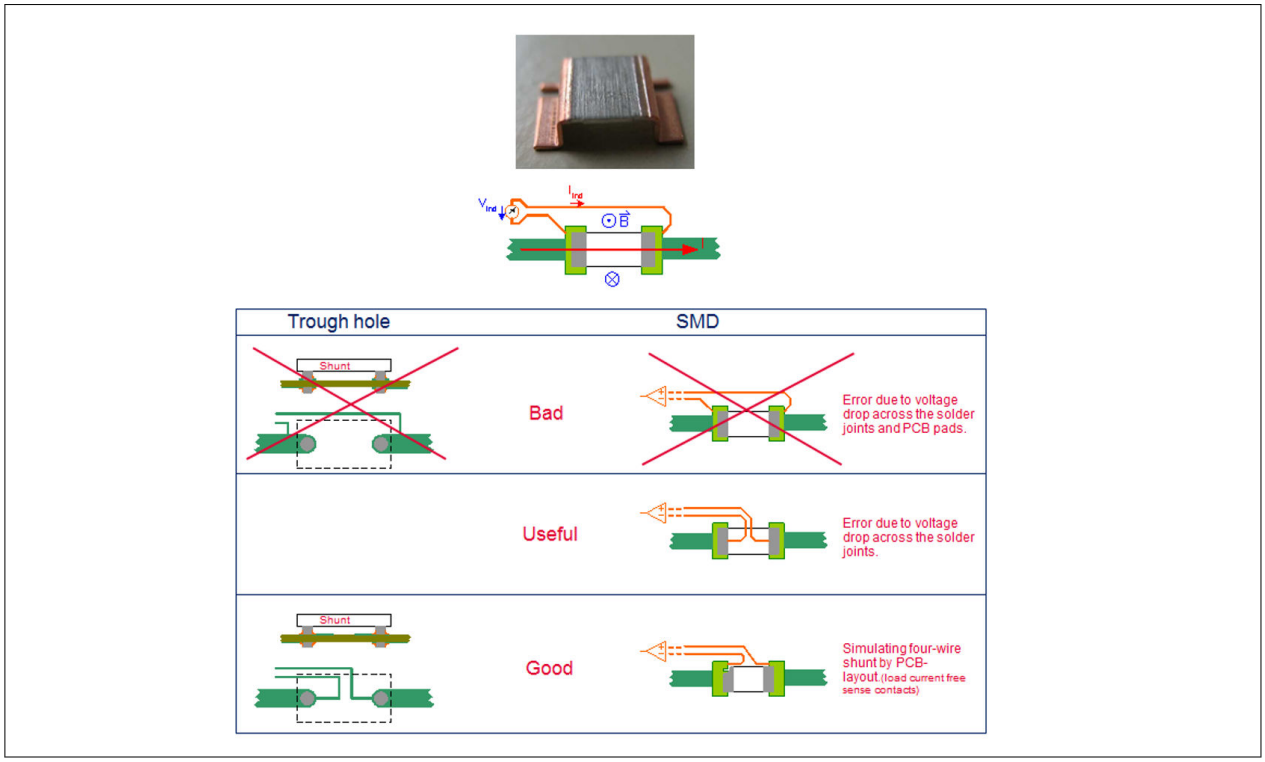


Figure 11 Layout recommendation – current sense shunt - none magnetic current sensing pseudo four wire technique

5 Revision history

Revision	Date	Changes
1.0	2020-03-06	Initial release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Edition 2020-03-06

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
IFX-ilq1570614472148

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury